SONY®

Training Manual

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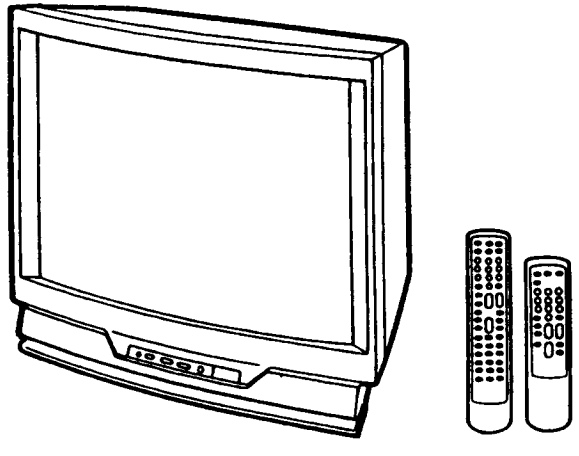
Color Television

AA-1/BA-1 Chassis

Circuit Description and Troubleshooting

KV-27TS36 / KV-20TS32

Course CTV-21



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Introduction

SONY has introduced a new modular line of TV chassis labeled the AA-1 and BA-1 chassis. The two chassis utilize PHILIP'S I^2C communications data bus for control of the internal chassis. They also share a common SONY main microprocessor and a common Y/C jungle IC to process video and generate deflection drive. Other features are a built-in closed-caption decoder IC and a newly designed dark tint trinitron picture tube.

The AA-1 chassis is used in all 27 and 32 inch screen size TV sets. The BA-1 is used in the 13 through 21 inch sets.

This manual begins by providing an overview of the AA-1 chassis. After that, detailed circuit analysis along with simplified drawings are provided on the AA-1. Since most of the circuits discussed are common to both chassis this manual provides only the major circuit differences for the BA-1 chassis. Additional troubleshooting hints, flowcharts and waveforms are provided to aid the technician in the repair of both chassis.

NOTE: Unless otherwise noted all voltages are measured with respect to chassis ground. During testing the TV was connected to an isolation transformer set to 117Vac and a color bar signal was input for a signal source. The instruments used are as follows:

FLUKE 8050A Multimeter.

VECTOR - VIZ ISO - V - ACII WP-30 Variac.

LEADER LCG-396 NTSC Pattern Generator.

AA-1 Chassis Block Diagram

A simplified block diagram of the AA-1 chassis is shown below. The major circuits are contained on the following boards:

UA Board Audio and video input/output terminals, audio and video switching, Y/C switching, comb filter and Y signal delay circuits.

A Board Main tuner (Audio MPX, VIF), sub tuner, and antenna switching.

M Board Main (system) microprocessor, audio processor (base and treble), variable audio amplifier, closed - caption decoder and Y/C jungle IC.

D Board Power supply, audio output amp, vertical drive and output, horizontal drive and output, pincushion modulation drive and output, x-ray protection module and flyback transformer.

Special features are added to upper line models by plug-in vertical boards to the set's D and UA boards. These are:

W Board Velocity modulation.

P Board Picture in Picture. This board connects onto the existing UA board.

E Board Dynamic convergence.

Operation

The ac line voltage is input to the power supply, on the D board, where it is noise filtered and rectified. The power supply generates the set's many regulated voltages. The main microprocessor, on the M board, communicates with the following ICs utilizing the I^2C data bus:

- Dynamic convergence IC.
- Y/C jungle IC on the M board.
- Picture in Picture (PIP) IC on the P board.
- Audio processor on the M board.

The main micon IC communicates with all other ICs from its output control ports and data, clock, and latch ports.

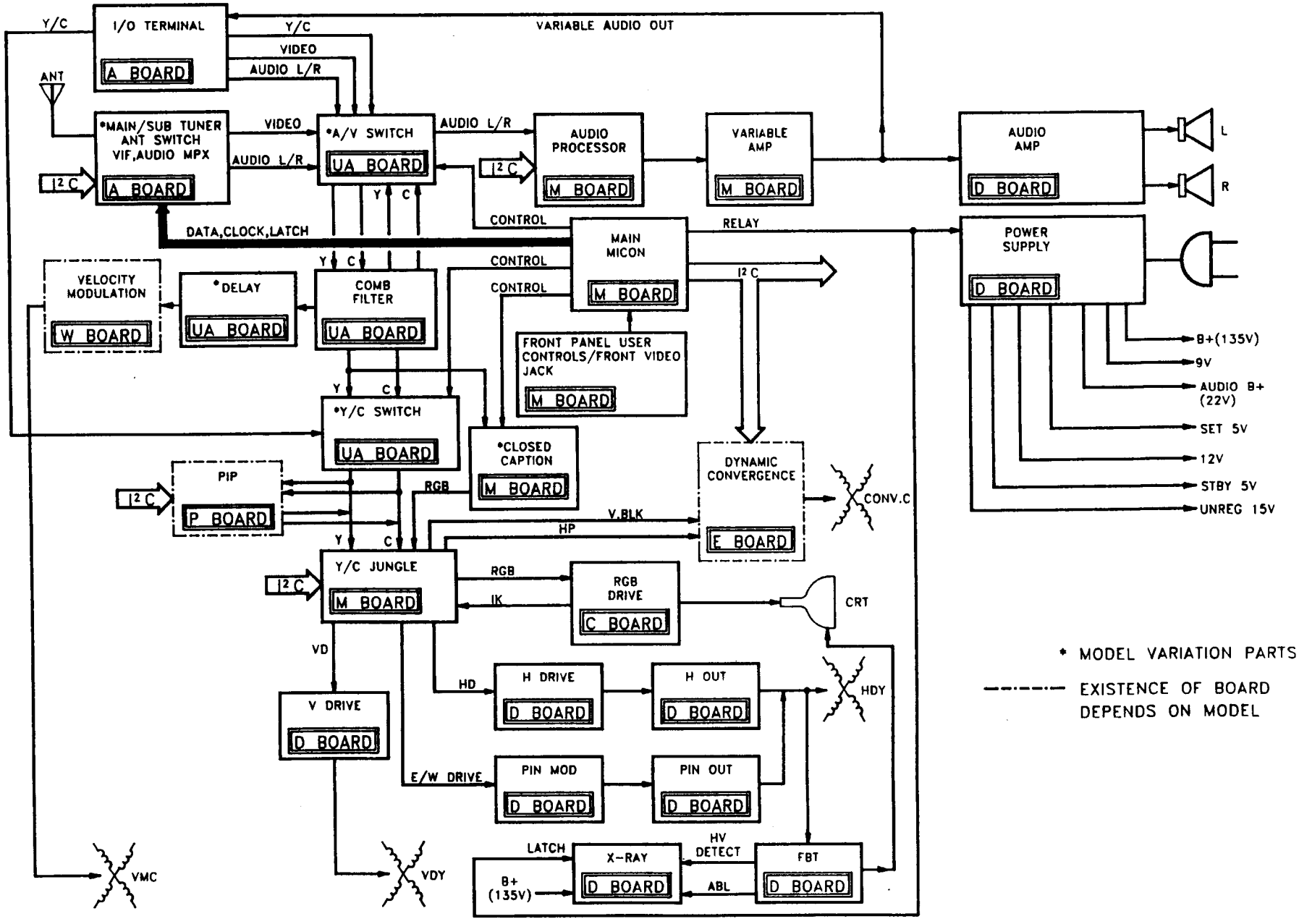
The main micon responds to key or SIRCS inputs from the user control H-board by communicating to the peripheral ICs via its output ports or I^2C data bus. In the case of video inputs, the main micon can select from various external I/O terminal inputs or the on board tuner. This is done by control signals sent to the A/V switch circuit on the UA board.

From the A/V switch, the selected video signal source is separated into Y (luminance) and C (chroma) components via either a glass or digital comb filter (depending on the tv model). Afterwards, the separated Y and C signals are input to the Y/C jungle IC. Additionally, depending on the tv model type, a separate Y/C switch circuit is utilized to switch the many external video inputs to the Y/C jungle IC.

The comb filter also outputs luminance signal information, via a Y delay, to the velocity modulation circuits on the W board. Likewise, the PIP circuit, on the P board, and the closed - caption circuit , on the M board, receive Y and C inputs from the comb filter (or from the Y/C switch in other sets), and outputs PIP Y and C signals to the Y/C jungle IC.

In addition to video signal outputs, the A/V switch selects L/R audio from the tuner and outputs these signals to the audio processor on the M board. From the audio processor circuit, the audio signals are sent to a variable audio amplifier. The variable audio amplifier outputs left/right audio signals to the audio output amp, to drive the speakers, and to the variable output jacks mounted on the I/O terminal board. The A/V switch also outputs left/right audio to the headphone's infrared amplifier mounted on the UA board.

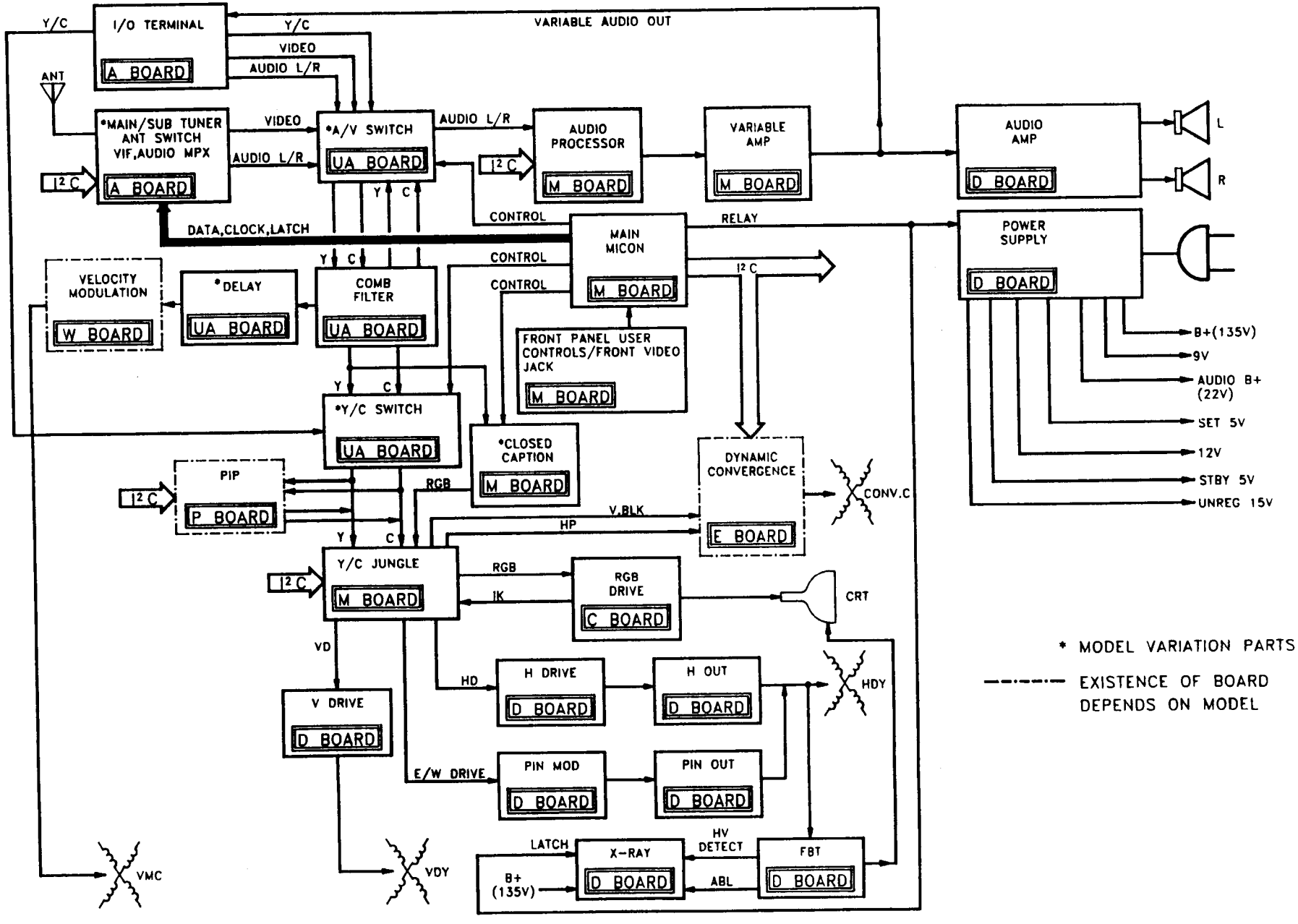
The Y/C jungle IC processes the Y and C input signals and outputs an RGB video signal to the CRT C board. It also outputs the east/west correction signal to the pincushion modulator, the vertical and horizontal drive signals to the deflection circuits, and the V. BLK and HP signals to the dynamic focus circuits on the E board.



AA-1 CHASSIS BLOCK DIAGRAM

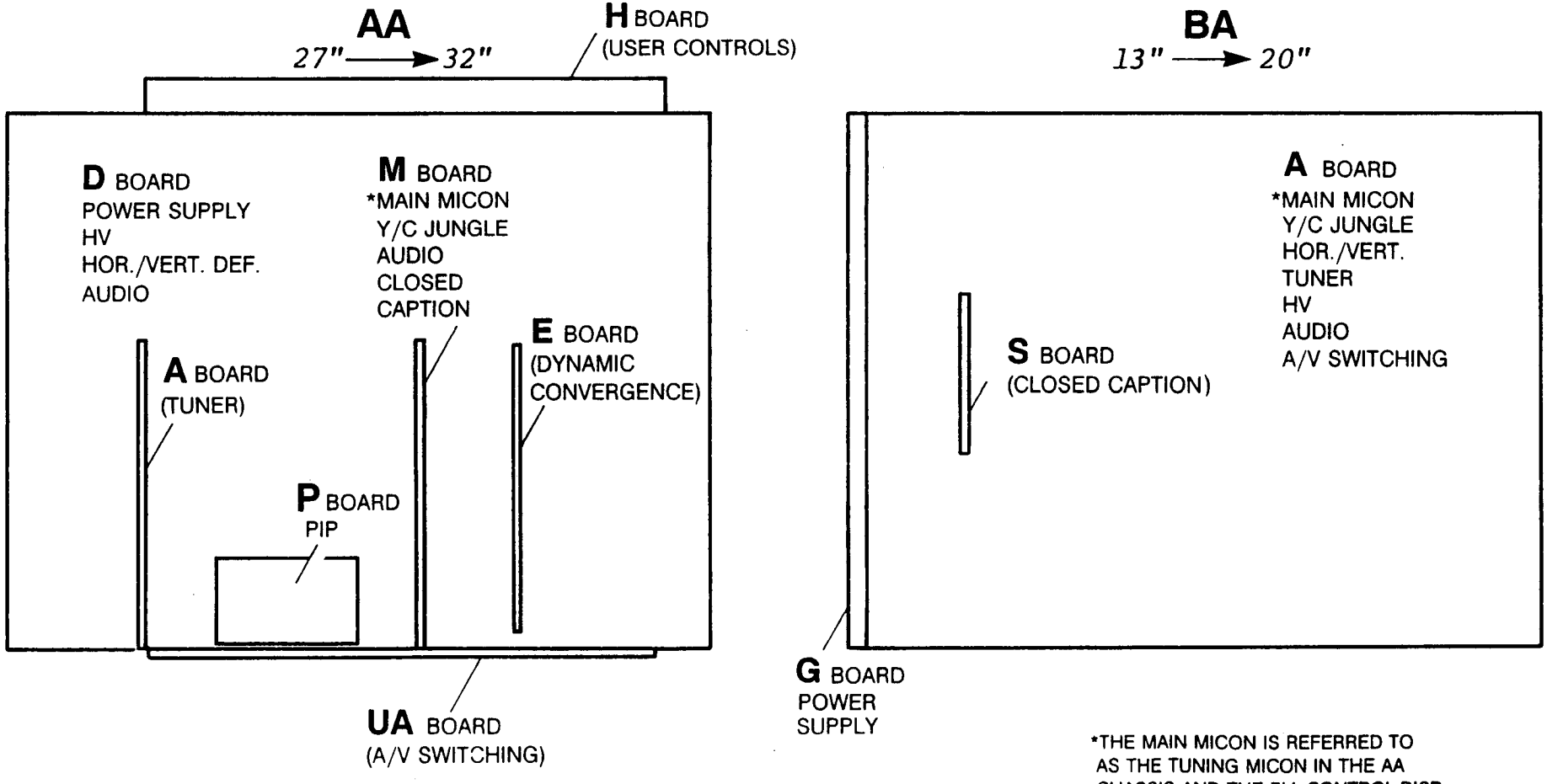
The horizontal deflection signal drives the flyback transformer which generates the high voltage to the CRT. In addition, the horizontal deflection signal is modulated with the east/west signal to correct for deflection system pincushion distortions.

The x-ray protection module monitors the high voltage system for abnormal high voltage conditions and to shut the set down.



AA-1 CHASSIS BLOCK DIAGRAM

NOTES



*THE MAIN MICON IS REFERRED TO AS THE TUNING MICON IN THE AA CHASSIS AND THE PLL CONTROL DISP. IN THE BA CHASSIS

AA-1 / BA-1 CHASSIS LAYOUT DIAGRAM

Power Supply Block

The AA-1 chassis power supply is comprised of the basic blocks shown below. These blocks can be divided into four separate sections. These are: Standby, Main Power, Regulation and Protection.

Standby 5V

The ac line input is filtered and is applied to the bridge rectifier, D602, and voltage doubler circuit, C607 and C608 to produce 315Vdc. This voltage is applied to two power converter transistors Q601 and Q602. The power converters alternately switch ON and OFF to allow current to flow through the CDT (constant drive transformer) T603 and the standby transformer T605. The standby transformer output is in turn rectified by D619 to produce unregulated 15Vdc. This voltage is then applied to the degaussing relay, RY601, and to IC602 to produce standby 5Vdc. The standby 5Vdc powers the main micon, IC101, while the set is OFF.

Main Power

To turn the set's main power ON, the main micon responds to inputs from the power ON switch, S1007, and the SIRCS detector IC101 (The power switch always has priority). The main micon will then output a relay drive signal via relay drive, Q604, to the power ON relay, RY602, which closes the relay contacts. When the relay contacts close, current flows through the power converters, the constant drive transformer and the power input transformer (PIT) T604. The resulting voltages produced by the PIT, (T604), are rectified to supply power to the set.

Regulation of the 135V Line

The 135Vdc is monitored by the control IC601 and control drive Q613. IC601 compares the 135 line voltage to a fixed internal voltage reference. As the 135 volts line varies (due to load changes) IC601 generates a control voltage that varies proportionally with load changes. This control voltage is applied to the constant drive transformer, T603, control winding. The control winding changes the ac efficiency of the constant drive transformer T603. Regulation is maintained by boosting or lowering the efficiency of the constant drive transformer with the varying load. Thereby, keeping the output levels of the power input transformer, T604, constant.

Protection

The 135 volt line is monitored by both an over current and over voltage (x-ray) circuit. In the figure, this circuit is represented by the x- ray and over current protector PM501.

Over Current

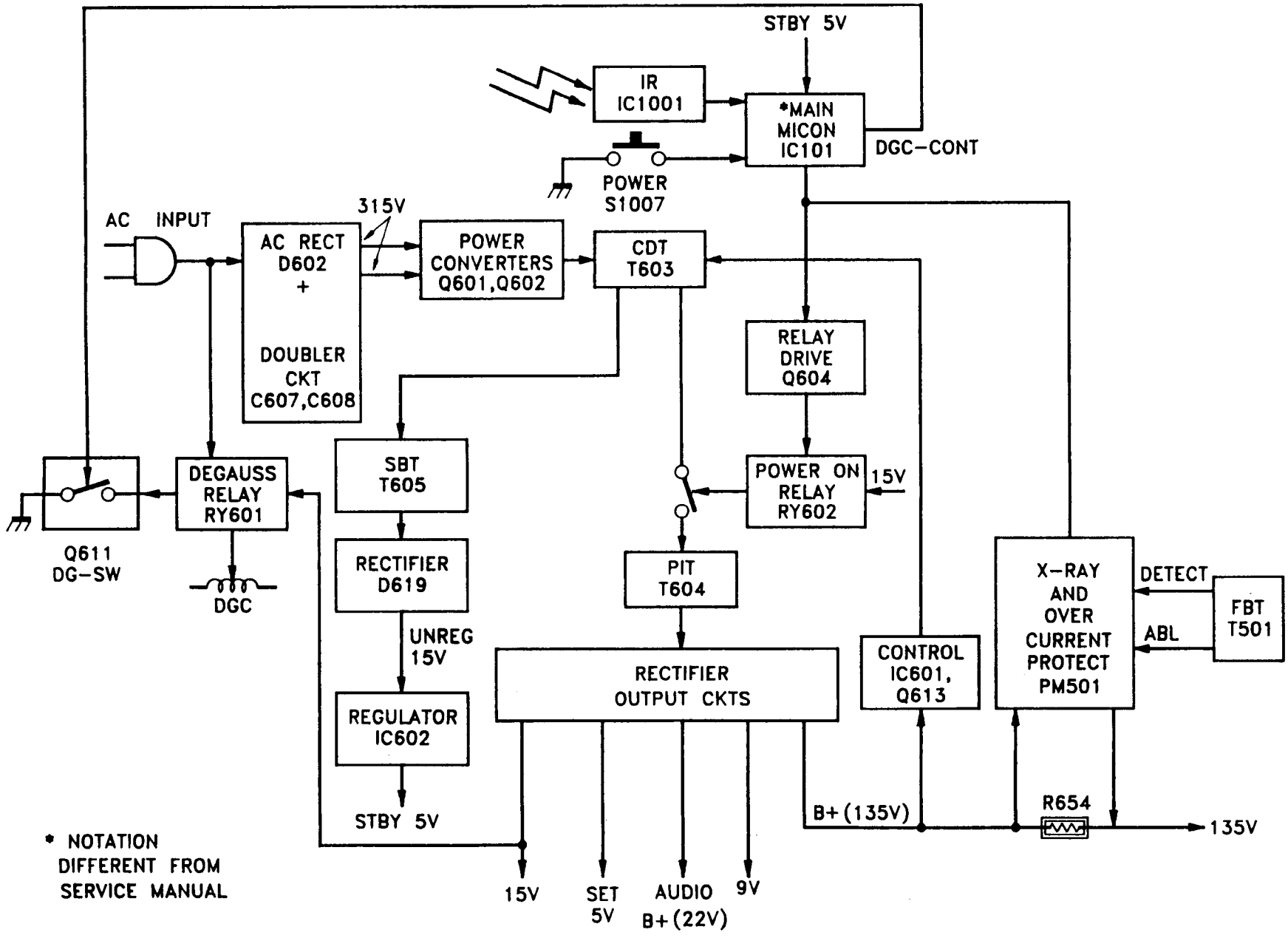
An over current condition is determined by the voltage drop across current limiting resistor R654. If a short or current overload occurs, on the 135 volts line, the voltage drop across the resistor will be enough to trigger the protection circuits within PM501. With the protection circuits triggered, the relay ON command will be shunted to ground de-energizing RY602. As a result, main power to T604 will be cut OFF and power to the set removed.

Over Voltage

Over voltage is determined by the voltage input to PM501 from the flyback transformer, T501, detect or ABL pins. If either high voltage (detect) or high current (ABL) is sensed, in the flyback system, the protection circuits within PM501 will trigger. The result is the same as mentioned earlier.

Degaussing

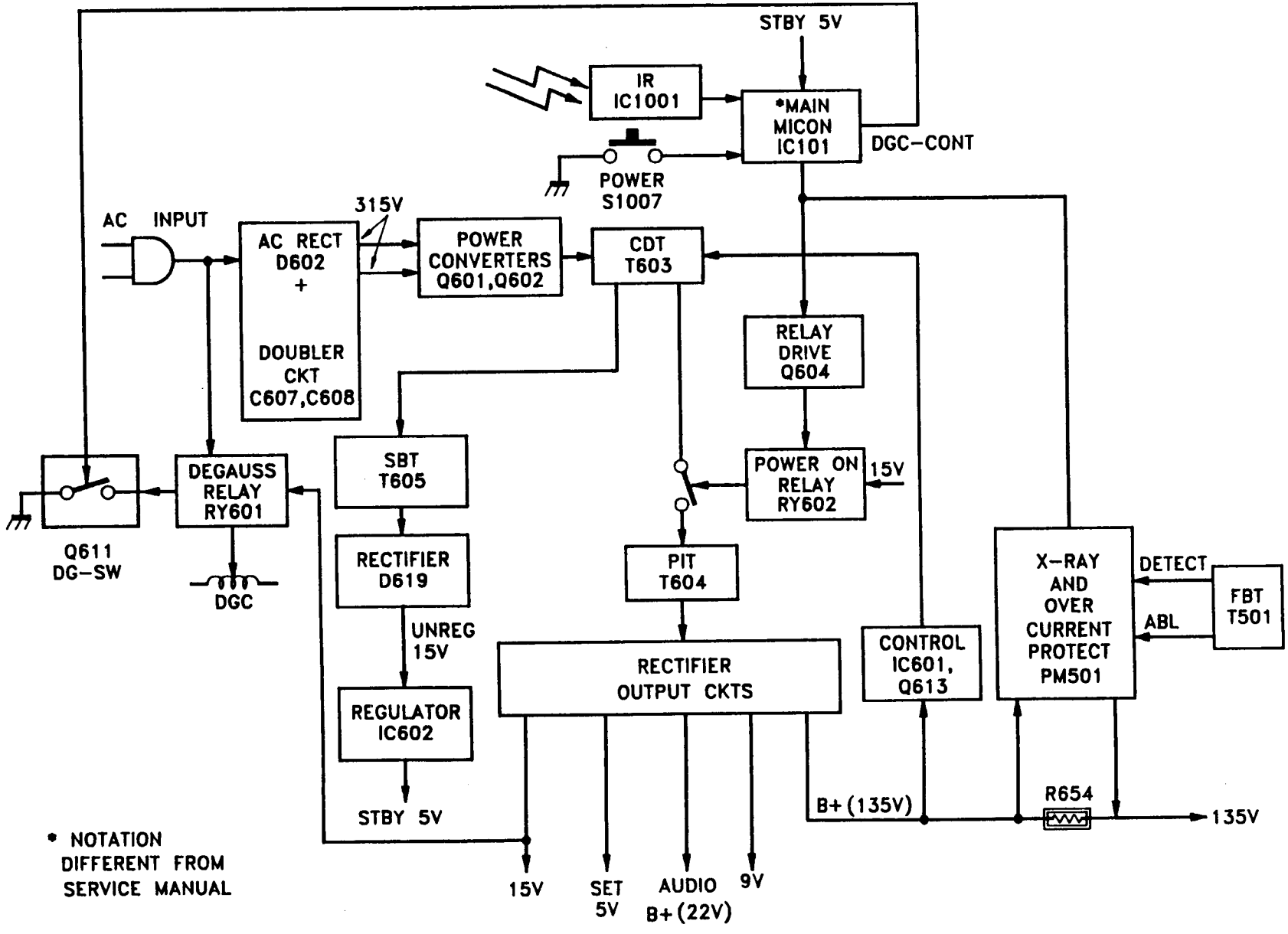
To degauss the CRT the main micon outputs a DGC-CONT signal to Q611 to turn Q611 ON. When Q611 turns ON current flows from ground through the degaussing relay, RY601, the 15Vdc supply, which closes the relay contacts. When the relay contacts close, ac current flows from the ac line through the degaussing coils to degauss the CRT. The DGC-CONT signal, output from the main micon, turns Q611 ON for a period of 4 seconds at power ON. Afterwards, the main micon turns Q611 OFF to stop current flow through the degaussing coils.



POWER SUPPLY BLOCK

BA-1 Chassis Degaussing

The BA-1 chassis does not use a degaussing transistor to control the degaussing of the CRT. In this chassis the degaussing relay, RY601, is driven from the PIT secondary rectified 16Vdc line. The other side of the degaussing relay is connected directly to ground. This allows the relay to be energized when the set is turned ON.



POWER SUPPLY BLOCK

AC Input / Degaussing

The power line is coupled through CN114, F601, line filters T601 and T602 to the bridge rectifier D602. The bridge rectifier and voltage doubling capacitors, C607 and C608, [illegible] the input ac line voltage to +315Vdc when measured across the anode and cathode of D602. When measured with respect to the ac power line neutral the cathode of D602 is +157Vdc and the anode is -157Vdc. The rectified +315Vdc sources the power converters Q601 and Q602. The power converters are discussed later.

The ac line is also connected to the degaussing coils through relay, RY601, degaussing switch transistor, Q611, and thermistor (positive temperature coefficient), THP601. When the set is turned ON, the main micon outputs a (HIGH) DGC-CONT signal to turn ON the degaussing switch transistor Q611. This activates relay, RY601, which allows ac current to flow through the thermistor and the degaussing coils. The DGC-CONT signal keeps Q611 ON for a period of 4 seconds. Thereafter, the main micon turns Q611 OFF to stop current flow through the thermistor and degaussing coils.

The thermistor in the degaussing circuit is used to gradually reduce current flow through the degaussing coils. Normally, this occurs within 1 second after current has been switched ON to the degaussing circuit. This action prevents the CRT from actually being magnetized rather than demagetized, which would occur if the current was suddenly cut-off to the degaussing circuit. The Q611 four second ON time period therefore ensures that a normal degaussing operation occurs.

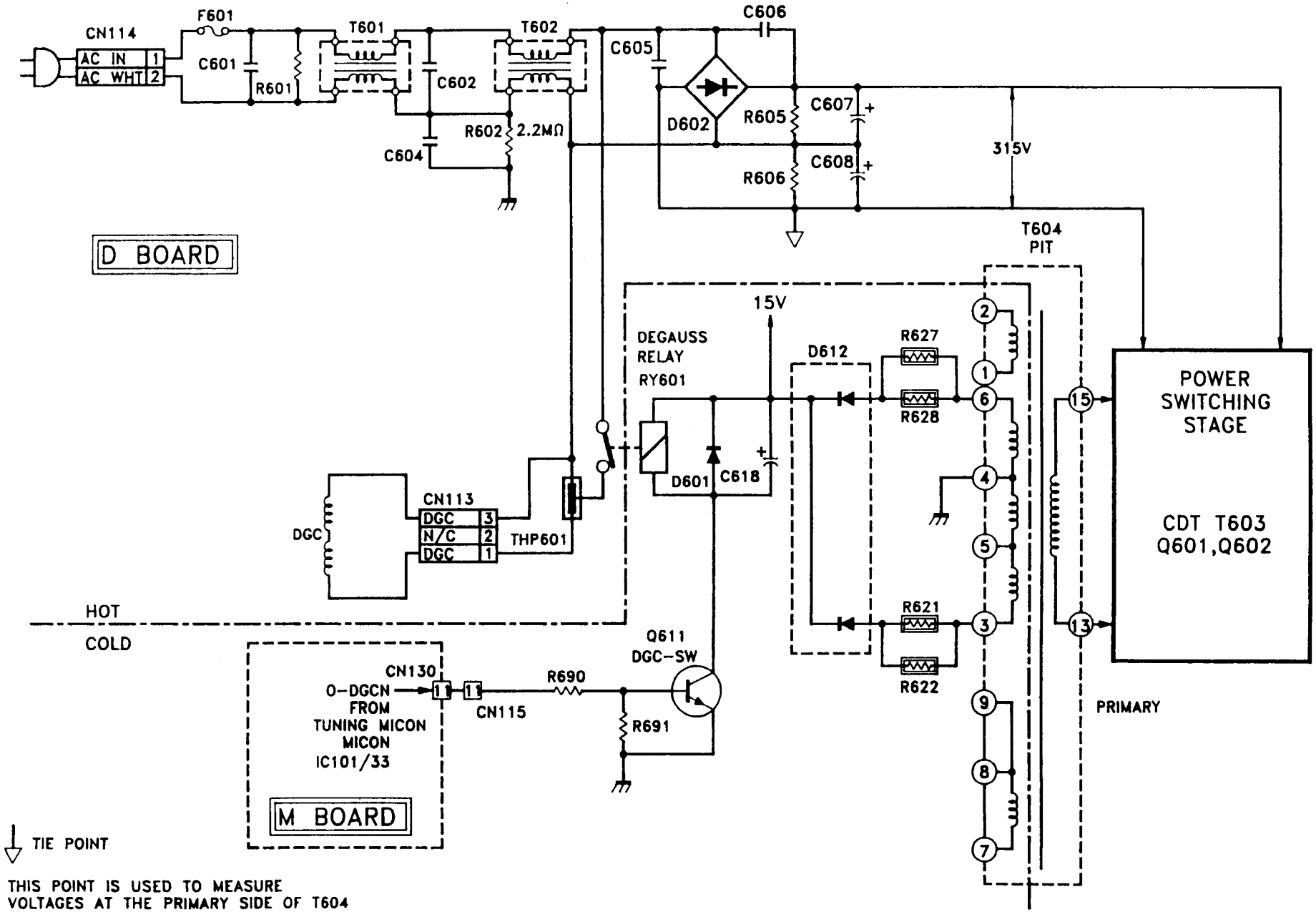
The degaussing switch Q611 circuit was designed into the AA-1 chassis for future considerations. With this circuit, it is quite possible for the user to degauss the CRT, at any given time, utilizing the remote control unit. This might easily be done by either pressing a function switch or selecting the degauss operation from the user menu screen.

Troubleshooting

WARNING! The set's chassis ground is isolated form the ac line. However, the power supply's input stage is at lethal ac potentials. You must use an isolation transformer prior to doing any type of troubleshooting to prevent bodily harm to yourself and damage to the set. Before replacing any parts, you must remove power and use the normal ESD measures to protect the electrostatically sensitive parts.

When troubleshooting for no power or dead set symptoms check the following:

Check the line fuse, F602, to ensure it passes the ac input line voltage to the bridge rectifier section, D602. If the fuse is opened, suspect the bridge rectifier,D602, filter capacitors C607 and C608 for shorts, and the power converters, Q601 and Q602 (in the following stage), for PN junction failure and for opened PIT, T604, windings.



AC INPUT / DEGAUSSING

Standby Power

The standby power supply is a switching type power supply. It consists of a constant drive transformer (CDT) T603, power converters Q601 and Q602, and a standby transformer (SBT) T605. The standby power supply produces both an unregulated 15Vdc supply, to the set's power ON relay, and to the reset/standby regulator IC602.

The standby power supply operates whenever the set is connected to the ac line.

Operation

As previously mentioned, the ac line is filtered, rectified, and voltage doubled to produce 315Vdc. The rectified 315Vdc is applied to the collector of Q601 and through R611 to the its base. Resistor R611 provides a slight forward bias to Q601. This immediately starts current flow from the anode of the bridge rectifier, D602, through the following components: C625, R644, SBT T605 pin 3 and pin 5, CDT T603 main windings pins 3 and 4, through Q601 emitter collector junction to the 315Vdc supply.

The initial circuit current flow starts the build-up of magnetic energy in the CDT. As result, a positive voltage is generated at T603 pin 6. This voltage is coupled through C609 and R609 to the base of Q601, turning Q601 ON. When Q601 turns ON it causes C625 to charge rapidly. When C625 is fully charged, it immediately cuts off the flow of current through the standby transformer, T605, the CDT, T603, and Q601. This action results in the immediate collapse of the build up of magnetic energy through the CDT and a negative voltage generated at T603 pin 6. As a result, Q601 turns OFF which completes the first half cycle of current flow through the CDT.

The collapse of magnetic energy through the CDT also generates a positive voltage at T603 pin 1. This voltage is coupled through C610, and R610 to the base of Q602, turning Q602 ON. When Q602 turns ON, C625 discharges through the following components: Q602 emitter collector junction, T603 pins 4 and 3, T605 pins 5 and 3, and R644. This completes the second half cycle of current flow through T603. Q601 will now turn ON again through the following components: C625, R644, SBT T605 pin 3 and pin 5, CDT T603 main windings pins 3 and 4, through Q601 emitter collector junction to the 315Vdc supply as described previously to maintain the oscillations.

The resonant frequency, in the standby mode, is approximately 55kHz determined by the capacitance of C609 and the inductance between the constant drive transformer T603 pins 6 and 5. The resonant frequency, in the power ON mode, is approximately 83kHz.

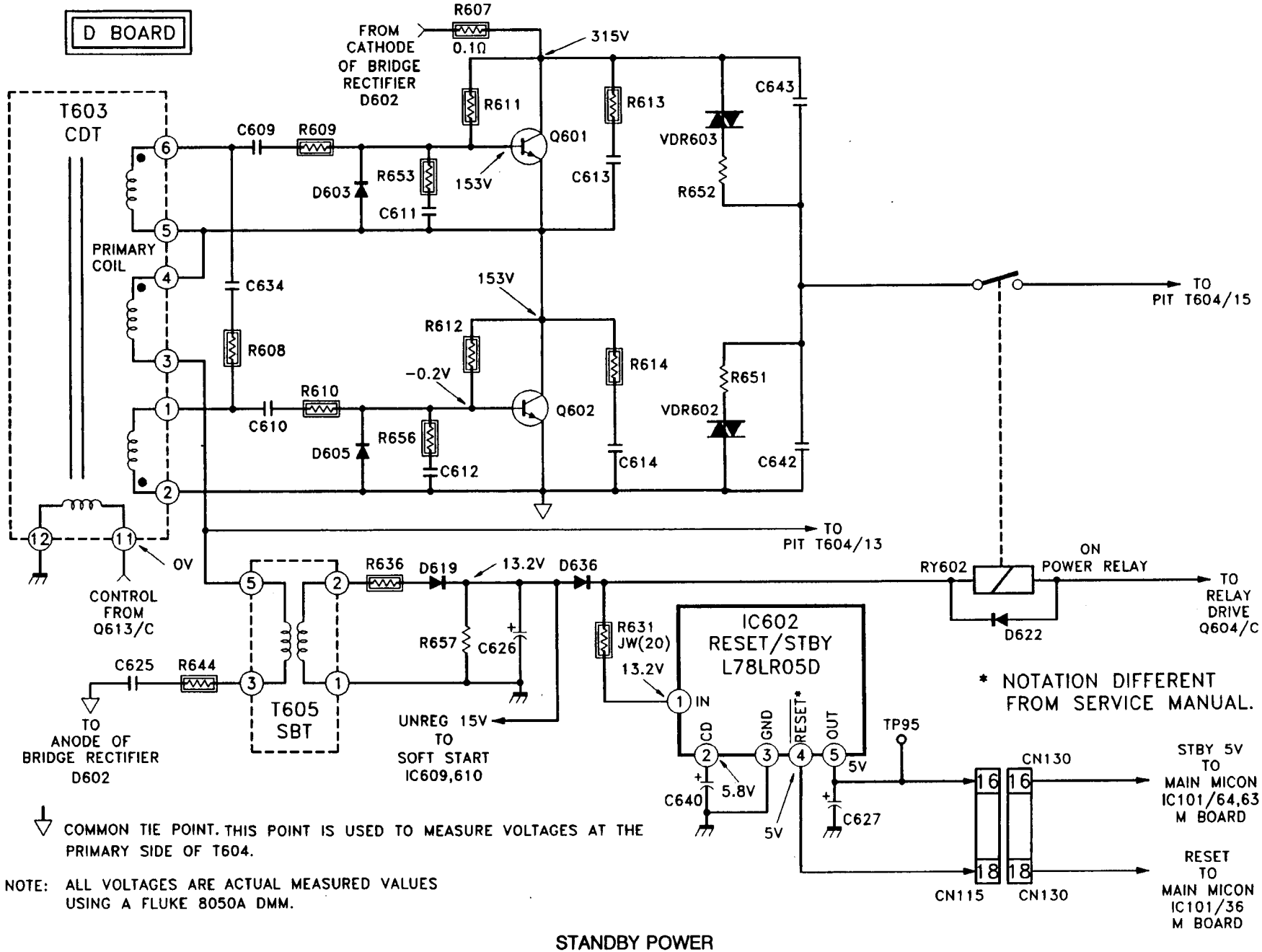
The inductance of the power input transformer, T604, (not shown) forms a parallel resonant circuit across the power converter circuit in the power ON mode. This forces the impedance of the main oscillation circuit to go down and the switching frequency to go up. This also results in a large current flow through C643, C642, the power converters Q601 and Q602. As a result, the voltage across both capacitors, C643 and C642, will increase. In order to prevent damage to the capacitors, they are clamped by two voltage dependent resistors VDR603 and VDR602. The VDR acts as a surge protector by bleeding the excess current across the capacitors when the VDR trigger point is exceeded.

As mentioned earlier Q601 and Q602 main current also flows through the primary windings of the standby transformer T605 pins 5 and 3. This current induces an ac voltage in the standby transformer secondary. The ac output from T605 pin 2 secondary is rectified by the half wave diode D619 and filtered by C626 to produce the set's unregulated 15Vdc supply (13.2Vdc measured). The resulting 13.2Vdc is coupled through D636 to the power ON relay, RY602, and to the reset/standby regulator IC602. The unregulated 15Vdc supply also sources soft start IC609 and IC610.

Relay, RY602, contacts close when the set is turned ON to apply switching power to the power input transformer, T604.

BA-1 Chassis Standby Power

The BA-1 chassis uses the same standby / reset regulator IC and has a similar switching power supply. Therefore, much of the power supply circuit operation and troubleshooting procedures will apply. The major difference between the two chassis is the physical location of the power supply. In the BA-1 chassis the power supply is located on a separated board labeled the G board.



STANDBY POWER

Troubleshooting

The AA-1 chassis ground is isolated from the ac line however, the power supply is not fully isolated from the ac line. Therefore, the use of an isolation transformer is essential when servicing the set. When troubleshooting for no power symptoms do the following:

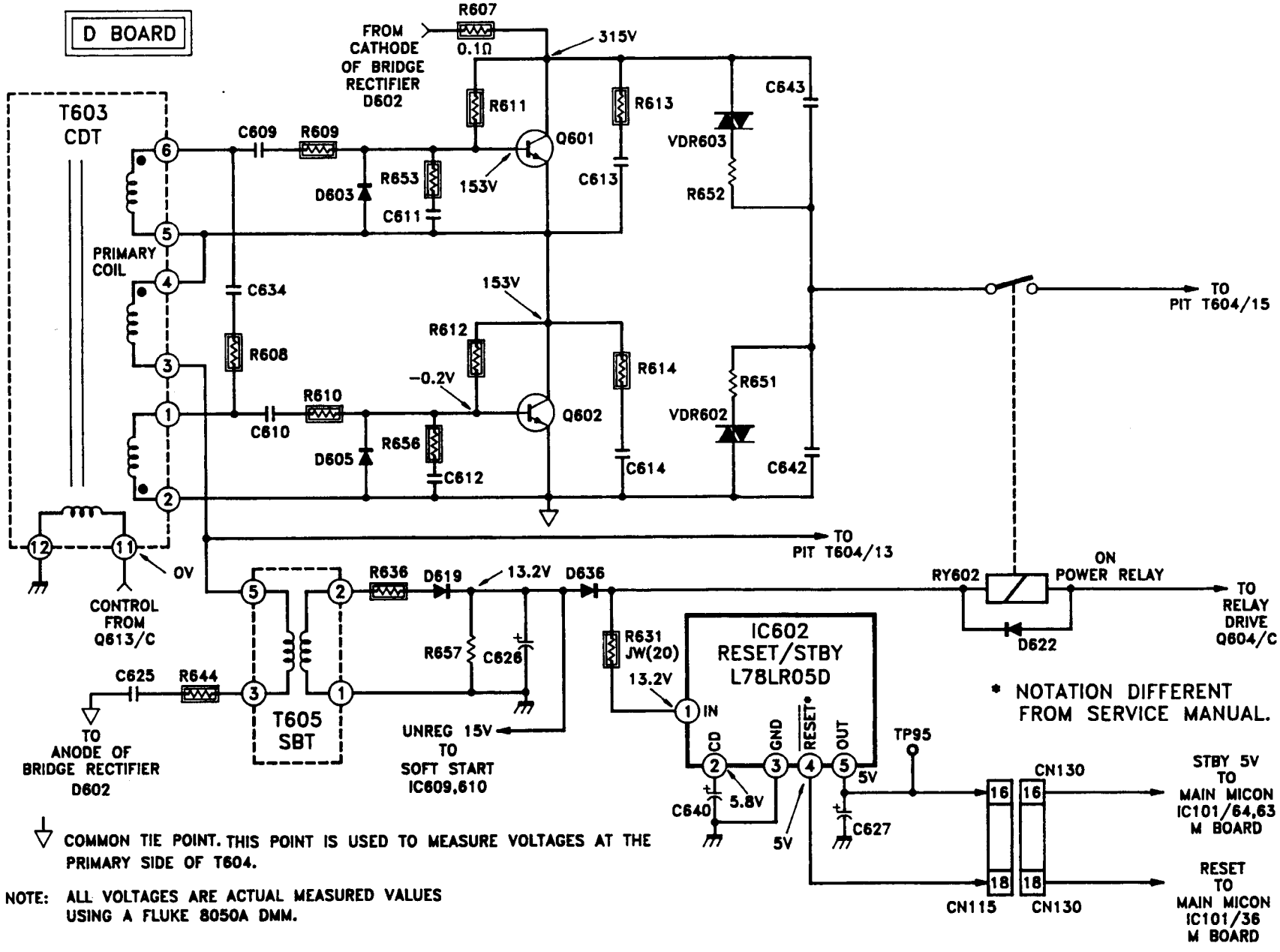
Check for 315Vdc at the collector of Q601 (measured from the emitter of Q602). If missing, suspect fuse resistor, R607, to have opened. If R607 is open, suspect Q601 and Q602 for PN junction failure. If Q601 and Q602 are defective, check diodes D603, D605, VDR603 and VDR602 for PN junction failure. Make the necessary repairs and proceed to do the following:

Set the oscilloscope to ac coupling and 50V/div. vertical deflection. Connect the oscilloscope probe to CDT T603 pin 3 and the ground probe to the emitter of Q602. Connect the set to an isolation transformer and variac. ***Do not turn the variac ON yet !*** Set the variac input voltage to 0Vac. Now turn the variac ON and slowly raise the input line voltage to 117Vac while observing the line fuse and the variac's current meter for any abnormal indications. If a current overload condition is detected, you still have a problem in either the ac input or power switching stage.

If okay, verify the normal switching frequency, input voltage, and current response are within those specified below:

AC Input	Switching Frequency	Volts Peak to Peak	Current
20Vac	71.5kHz	55.4Vp-p	< 0.1A
40Vac	71.5kHz	105Vp-p	< 0.1A
60Vac	71.5kHz	159Vp-p	< 0.1A
80Vac	65.5kHz	213Vp-p	< 0.1A
100Vac	59.5kHz	274Vp-p	< 0.1A
120Vac	56.5kHz	331Vp-p	< 0.1A
130Vac	57.1kHz	359Vp-p	< 0.1A

If okay, and the set will not power ON, check for unregulated 13.2Vdc at IC602 pin 1 and for regulated 5Vdc at IC602 pin 5. If either the 13.2 or 5 volts is missing, troubleshoot around the respective circuits.



STANDBY POWER

Power ON

The main power supply uses the same switching circuits described in the standby power supply section for main power. The main power supply consists of a constant drive transformer (CDT) T603, power converter transistors Q601 and Q602, and power input transformer (PIT) T604. The operation of the switching power supply was described in the previous section labeled standby power. This section will only describe the events that pertain to the operation of the main power supply.

Operation

To turn power ON, the main micon, IC101, responds to a LOW (0vdc) from the power ON switch, S1007, or SIRCS data from the sircs sensor IC1001 pin 1. IC101 pin 4 outputs a HIGH (5Vdc) through R009, CN131, CN116, R632, D628, R639 to produce 0.8Vdc at the base of relay drive Q604. Q604 turns ON causing current to flow from the standby transformer, T605 pin 2 (not shown), relay RY602 energizing the relay to close its contacts.

When the relay contacts close, current flows from the power switching stage comprised of CDT, T603, and power converter transistors, Q601 and Q602, to the power input transformer (PIT), T604, pins 13 and 15. The PIT primary current flow induces current flow in its secondary. The voltages generated from the secondary of the PIT powers the set's many circuits. These are discussed later on.

Protection

The function of the shutdown circuits is to safeguard the set in the event of a power supply or high voltage stage malfunction. In the event this occurred, a protection circuit triggers to cut OFF main power to the set. Normally, this is done by grounding the relay drive signal, at the anode of D628, through R645 and the protection module, PM501 (not shown).

During normal operation the voltage present at the anode of D628 is 2.8 Vdc. If a malfunction occurs, the voltage at the anode is immediately pulled LOW (0.7Vdc). The voltage at the base of Q604 now will be brought to 0Vdc due to the series voltage drop through D628, R639 and R638, which turns Q604 OFF. When Q604 turns OFF it de-energizes the relay causing its contacts to open. As a result, power to the PIT is cut OFF. The standby power supply however, will continue to function and the protection latch will remain triggered. The protection latch circuit may be reset by disconnecting the set from the ac power line or by pressing the power button again on the remote or the front panel of the set.

Troubleshooting

When troubleshooting a no power ON condition (dead set), first verify the operation of the standby unregulated 15Vdc and 5Vdc supply sections. Also look closely at the items that appear to work, such as relay click noise, the presence of CRT filament lighting, etc.. Much of this information will save you troubleshooting time. If the standby power supply section is operating but the sets secondary voltages are missing, then do the following checks:

- Apply ac power. Turn the set ON and verify that there is 0.8Vdc at the base of Q604. If okay, check for 0.3Vdc at the collector. If missing, check the relay for continuity. Suspect also the relay contacts.

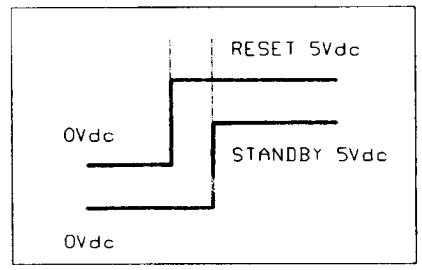
If 0.8Vdc is missing at the base of Q604 do the following:

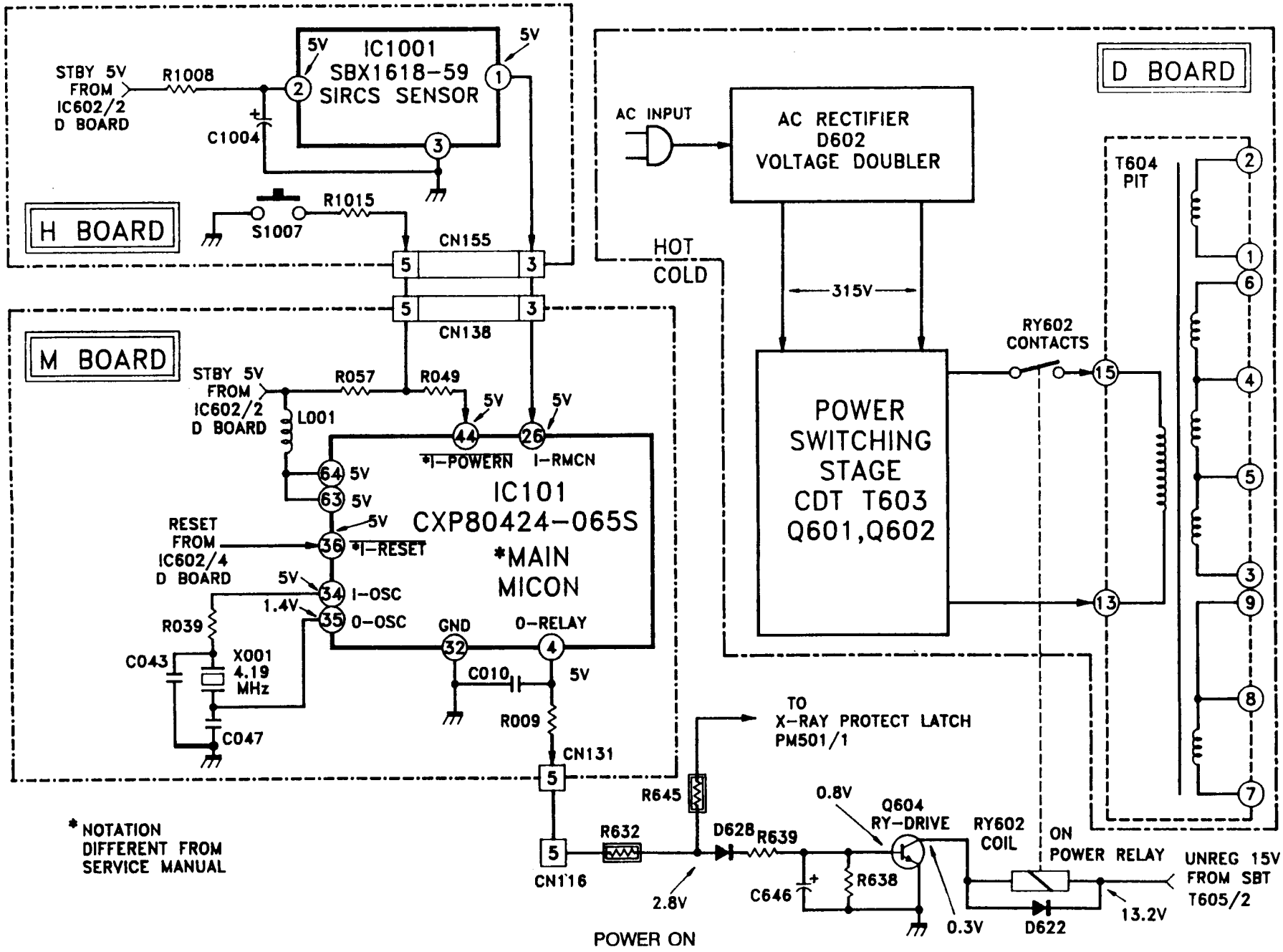
- Verify that there is 2.8Vdc at the anode of D628. If less than 2.8Vdc suspect the x-ray protect latch to have triggered. Go on to troubleshooting that section.

- Check for 5Vdc at connector CN116 pin 5. If missing, troubleshoot the main micon, IC101, on the M board. While there verify the following:

- Standby 5Vdc at IC101 pins 64 and 63.

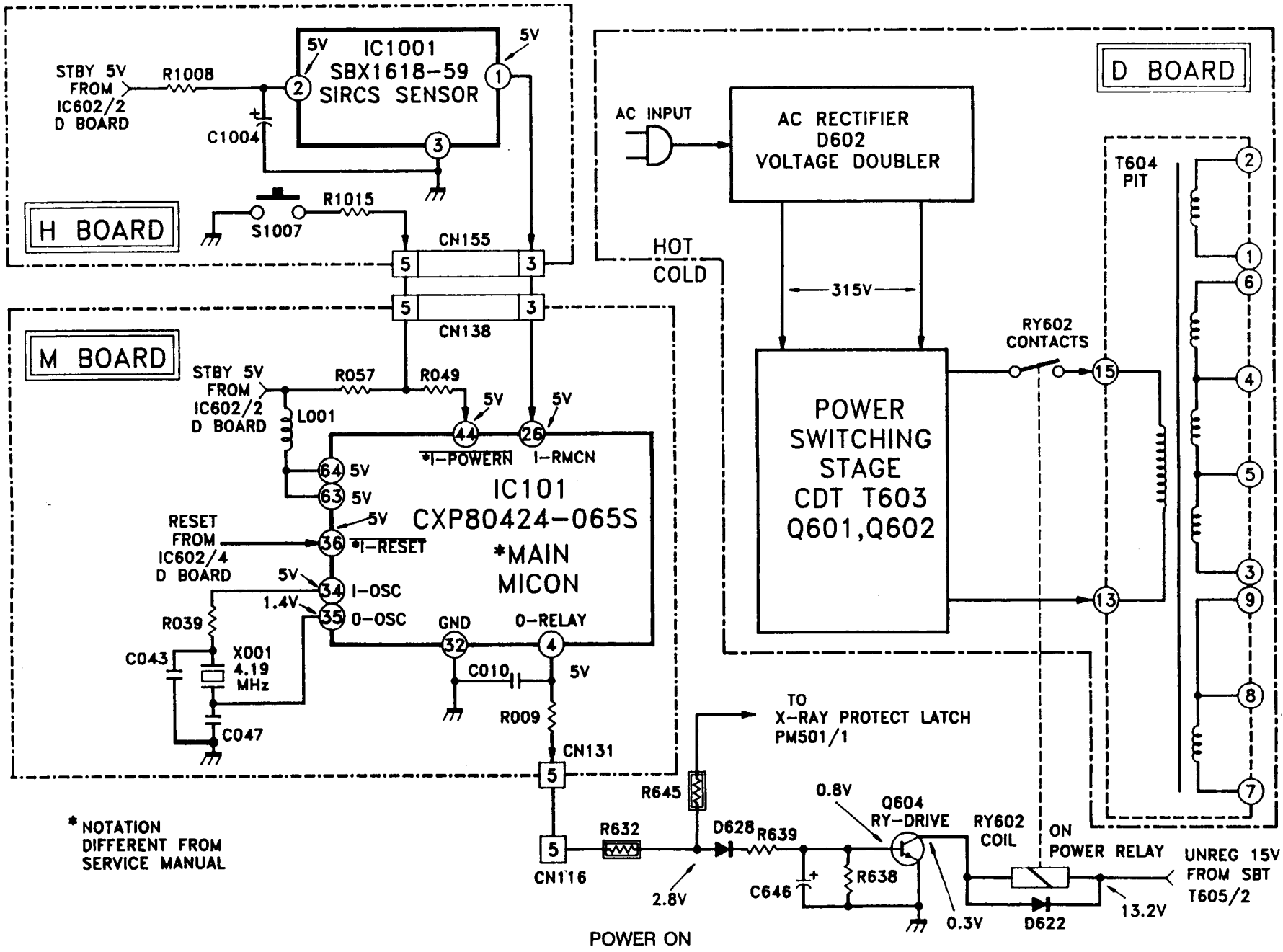
- Reset at IC101 pin 36. This is 0Vdc rising to 5Vdc (delayed with respect to the standby 5Vdc supply line) at ac plug in. Reset is shown in the figure below.




H BOARD
M BOARD
D BOARD
STBY 5V FROM IC602/2 D BOARD
R1008
C1004
IC1001
SBX1618-59
SIRCS SENSOR
5V
R1015
S1007
CN155
CN138
AC INPUT
AC RECTIFIER
D602
VOLTAGE DOUBLER
HOT
COLD
315V
POWER
SWITCHING
STAGE
CDT T603
Q601,Q602
RY602
CONTACTS
T604
PIT
R057
R049
L001
*I-POWERN
I-RMCN
IC101
CXP80424-065S
*MAIN
MICON
RESET FROM IC602/4 D BOARD
*I-RESET
I-OSC
O-OSC
1.4V
R039
C043
X001
4.19
MHz
C047
GND
O-RELAY
C010
R009
CN131
TO
X-RAY PROTECT LATCH
PM501/1
R645
0.8V
Q604
RY-DRIVE
RY602
COIL
ON
POWER RELAY
UNREG 15V
FROM SBT
T605/2
R632
D628
R639
CN116
2.8V
C646
R638
0.3V
D622
13.2V
POWER ON
* NOTATION
DIFFERENT FROM
SERVICE MANUAL

Note: If reset does not occur, the set will operate and the microprocessor will function normally. On the other hand, if reset is held LOW (0Vdc), the main micon, IC101, will not function however its crystal will run.

- 4.19MHz 4.2Vp-p clock signal at pins 35 and 34.
- LOW (0Vdc) at pin 44 when the power button is pressed or LOW going SIRCS data at pin 26 when the remote control power button is pressed.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RESET
FROM
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D BOARD
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I-OSC
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1.4V
R039
C043
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4.19
MHz
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O-RELAY
C010
R009
CN131
TO
X-RAY PROTECT LATCH
PM501/1
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0.8V
Q604
RY-DRIVE
RY602
COIL
R632
D628
R639
CN116
2.8V
C646
R638
0.3V
D622
ON
POWER RELAY
13.2V
UNREG 15V
FROM SBT
T605/2
* NOTATION
DIFFERENT FROM
SERVICE MANUAL
POWER ON

Regulation / Soft Start

The power supply regulation circuit, IC601, compensates for the ac input line voltage fluctuations and power input transformer (PIT), T604, secondary load variations so that the secondary output voltages remain constant. Regulation is done by varying the power input to the PIT. Controlling the power input to this stage will determine the output voltage levels at the secondary of T604.

To regulate, IC601 pin 1 samples the B+ (135Vdc) line and uses this sample to output a control voltage from pin 3. This voltage is then used to vary current flow through the CDT,T603, control winding pins 11 and 12 via the control drive transistor, Q613. IC601 internally is comprised of a three terminal programmable shunt regulator. The standard circuit is shown in the diagram. The circuit operation is explained below.

Operation

The power regulating transformer is cross-wound. That is, it has a control winding wound at right angles to the main windings. In the diagram, the control windings are connected between T603 pins 11 and pin 12.

The characteristics of the CDT is such that current flow through the control winding changes the efficiency of the CDT. The efficiency of the CDT varies inversely with the current flow through the control winding. In other words, a current rise through the control winding decreases the efficiency of the CDT. Conversely, a current decrease, through the control winding, increases the efficiency of the CDT. As a result, input power to the PIT, T604, can be controlled with the CDT control current.

The B+ (135Vdc) supply line is coupled through R635 to IC601 pin 1. Therefore, any fluctuations in the B+ (135Vdc) supply line is sensed at IC601 pin 1. The fluctuations, in the 135Vdc line, are processed through the IC, which results in a control voltage to be generated from pin 3. The output, from IC601 pin 3, is coupled through R633 to the base of Q613. Q613 is biased by the 16Vdc supply derived from T604 pin 3 through R622, R621, D602, C618 and D627.

The operation of IC601 when the 135Vdc line decreases is as follows:

- Voltage at IC601 pin 1 decreases.
- The control voltage output from IC601 pin 3 increases.
- Q613 turns ON less which causes the CDT, T603 pin 11, control current to decrease.
- The CDT's efficiency increases (the switching frequency goes down).
- This increases the power input to the PIT, T604, which raises the secondary output voltages.

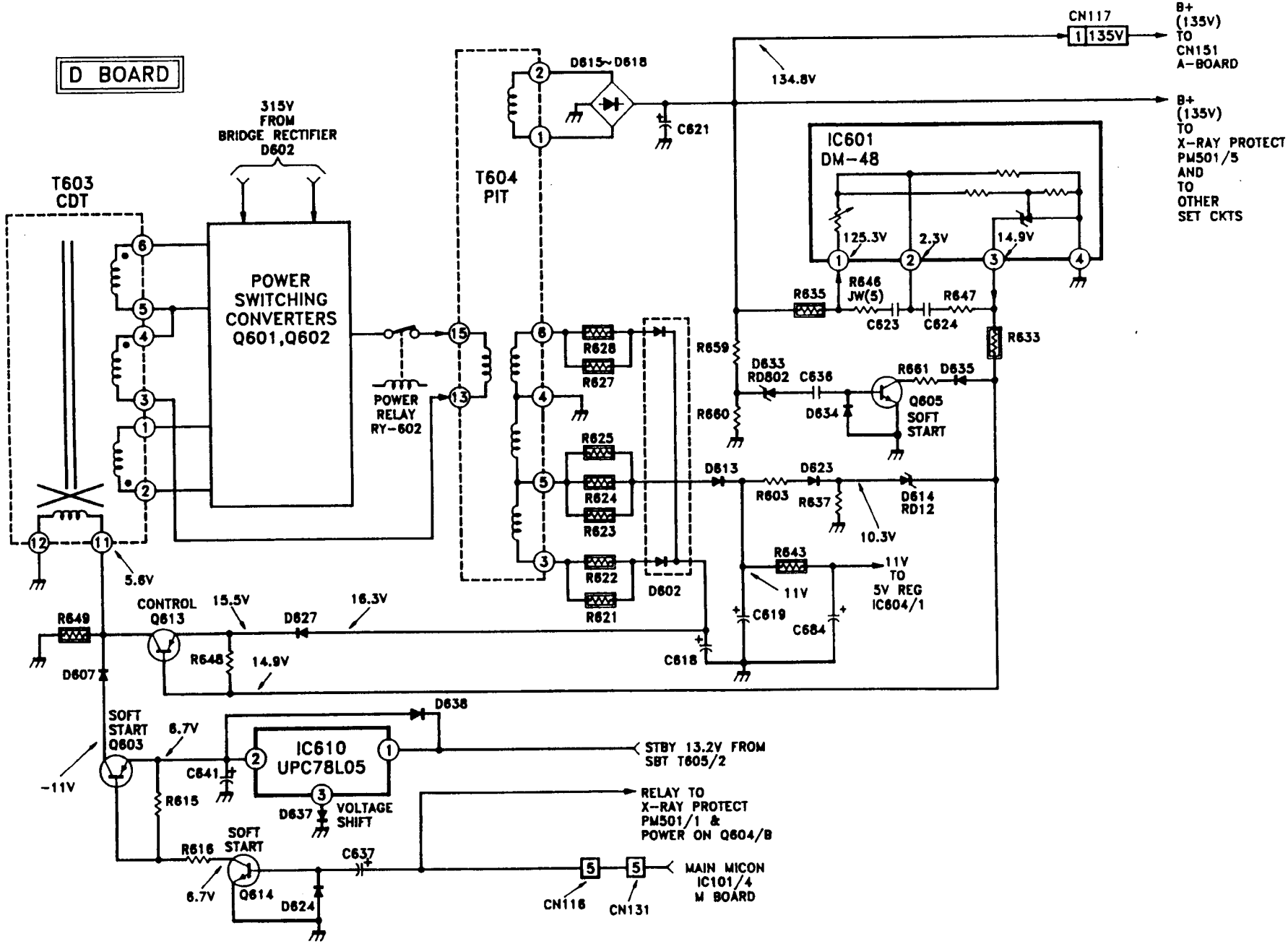
The opposite occurs if the 135Vdc secondary line should increase.

Soft Start

The soft start circuit reduces the initial current surge, through the power switching converter transistors, as the filter capacitors in the PIT's secondary charge up at power ON. It also prevents false triggering by the protection circuits when power is turned ON.

Q603, Q614, IC610 and C637 comprise the soft start circuit. When power is turned ON, the main micon, IC101 pin 4, outputs 5 volts through C637 to the base of the soft start transistor Q614. Q614 turns ON for the period determined by the time constant of C637 and the Q614 base to emitter junction resistance. When Q614 turns ON it turns Q603 ON. This allows current to flow from chassis ground through the CDT, T603, pins 12 and 11, D607, Q603 collector to emitter junction to the standby power supply IC610.

The current flow through the CDT, T603, control winding decreases the efficiency of the CDT and the power input to the PIT for the period Q614 and Q603 are turned ON. As C637 gradually continues to charge, the voltage applied to Q614 and Q603 is reduced causing Q614 and Q603 to turn ON less. This causes less current to flow through the CDT control winding which increases the efficiency of the CDT. As a result, this increases the input power to the PIT which raises the secondary output voltages.



REGULATION / SOFT START

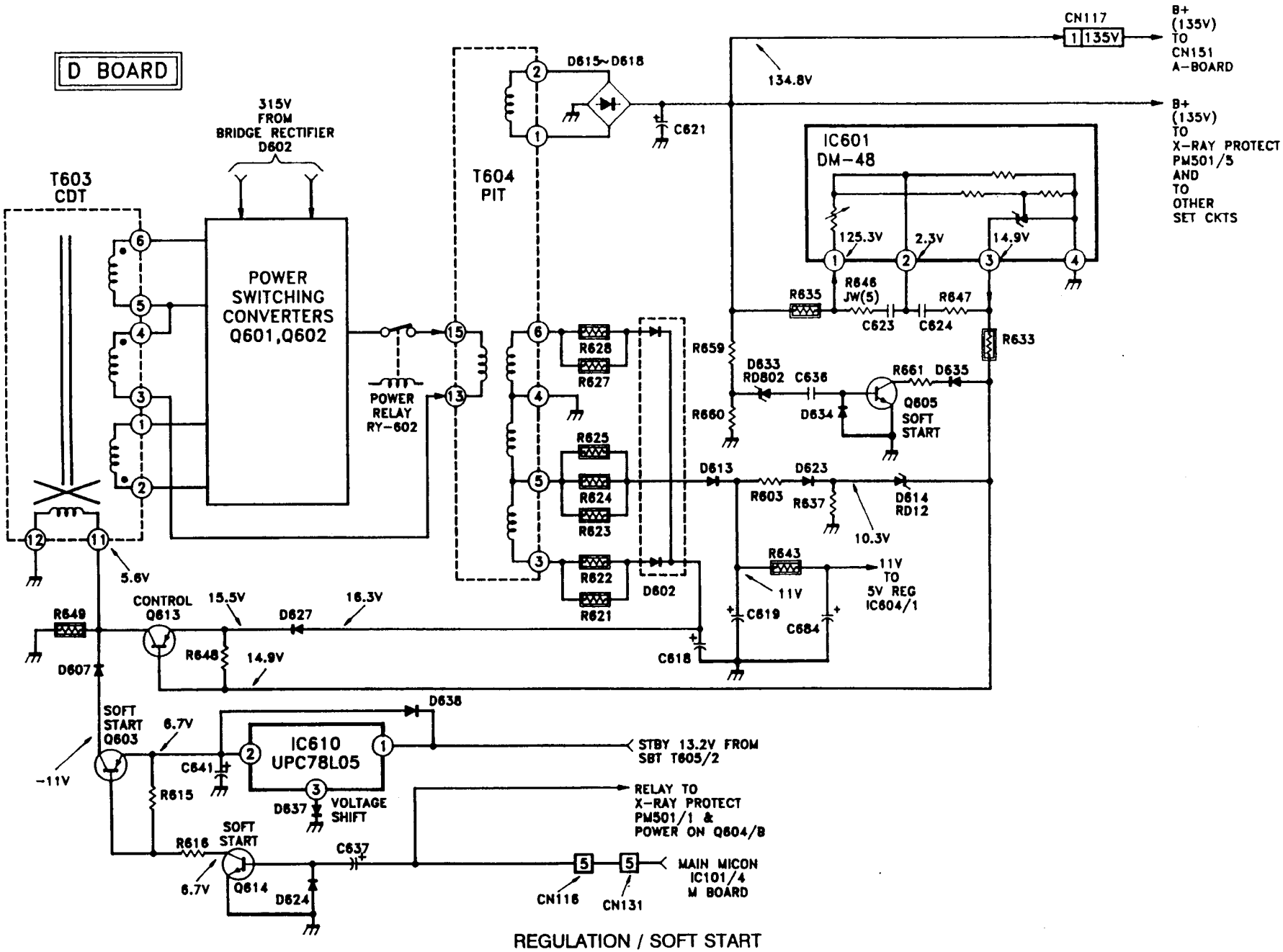
Troubleshooting

As previously mentioned, the power supplies regulator, IC601, and associated circuitry, function in a close loop manner to maintain precise and stable regulation. As a result, troubleshooting intermittent power supply shutdown problems or regulation problems can be difficult. The steps outlined below will allow you to perform basic power supply checks and roughly confirm safety related hold-down voltage checks by temporarily defeating the regulation control loop:

- Open the regulation control loop by unsoldering T603 pin 11 from the circuit.
- Tack solder the cathode end of a 1A rectifier diode to T603 pin 11 terminal. **NOTE:** The diode is needed to block ac feedback from the CDT T603 pin 11 to the external power supply you hook-up in the following step.
- Connect the other end of the diode to a variable dc power supply source. Then set the external power supply voltage to 5.2Vdc. Note: This voltage must be set to 5.2Vdc to allow the set to turn ON and prevent shutdown at power ON.
- Connect the ac supply line to a variac and isolation transformer combination and set the ac input line voltage to 79Vac.
- Turn the set ON. If the switching power supply is working the TV should power up.
- Now raise the external power supply voltage to 5.6Vdc.
- Then slowly raise the input line voltage to 117Vac while observing the voltage at CN117 pin 1 (measured from chassis ground). ***DO NOT ALLOW THIS VOLTAGE TO GO ABOVE 135Vdc!***
- Slowly raise the external input dc supply voltage while observing the voltage at CN117 pin 1. The voltage at CN117 pin 1 should now decrease.
- Slowly lower the external input dc supply voltage while observing the voltage at CN117 pin 1. The voltage at CN117 pin 1 should now increase.
- If you continue to lower the external supply voltage you will be able see the voltage, at CN117 pin 1, that will place the set into x-ray protect. This voltage should be approximately 137Vdc when the raster disappears. Remember, this is an approximate rough check and is not intended to replace any safety procedural checks outlined in the service manual.

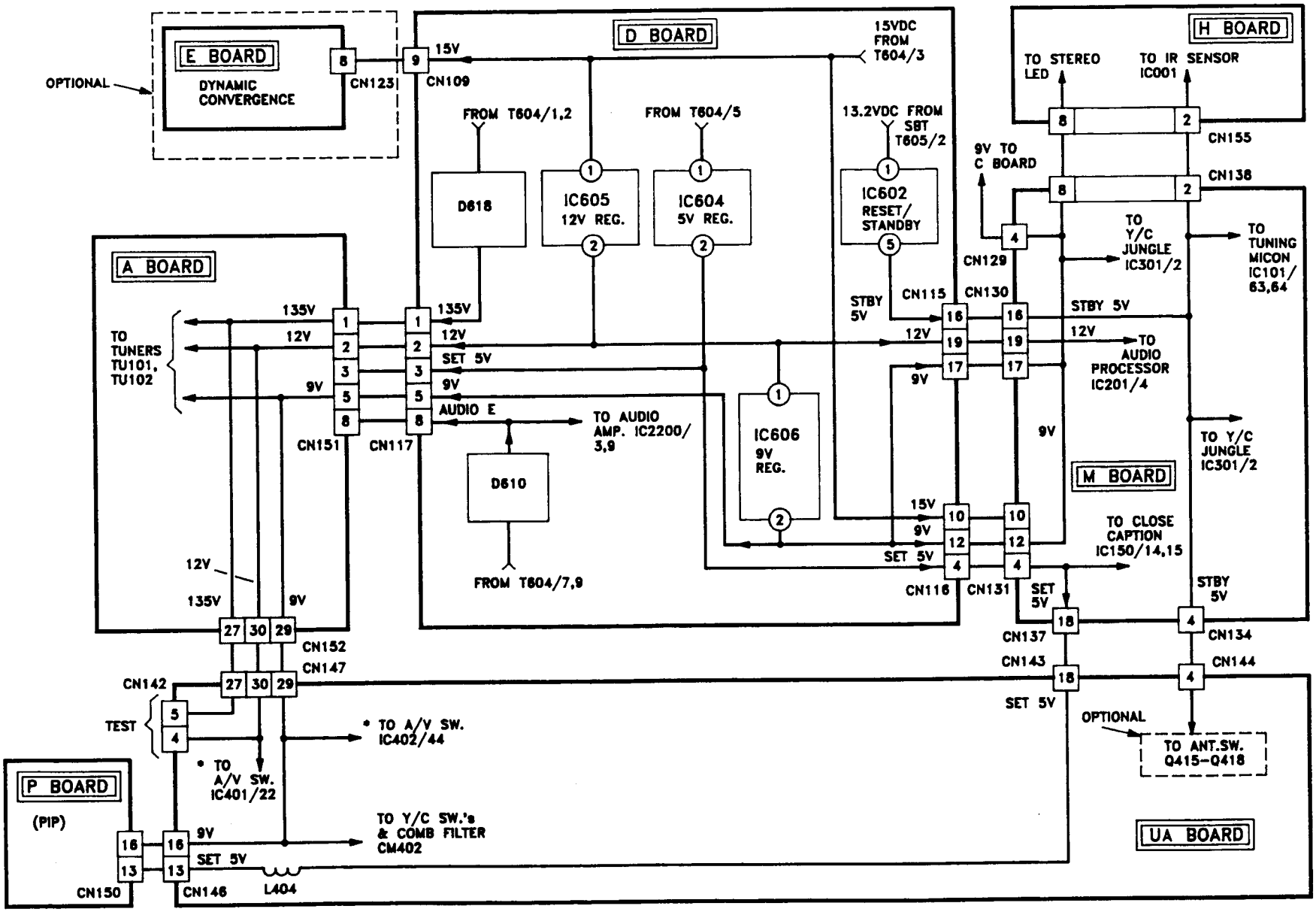
With the regulation control loop opened, you will be able to do basic voltage checks around the regulation stage while preventing the set from going into shutdown.

B+ (135Vdc) line output voltage when T603 pin 11 is fixed to 5.6 Vdc	
Input AC voltage	**B+ (135 volt line)**
80Vac	82Vdc
90Vac	92Vdc
100Vac	106Vdc
110Vac	120Vdc
120Vac	134Vdc



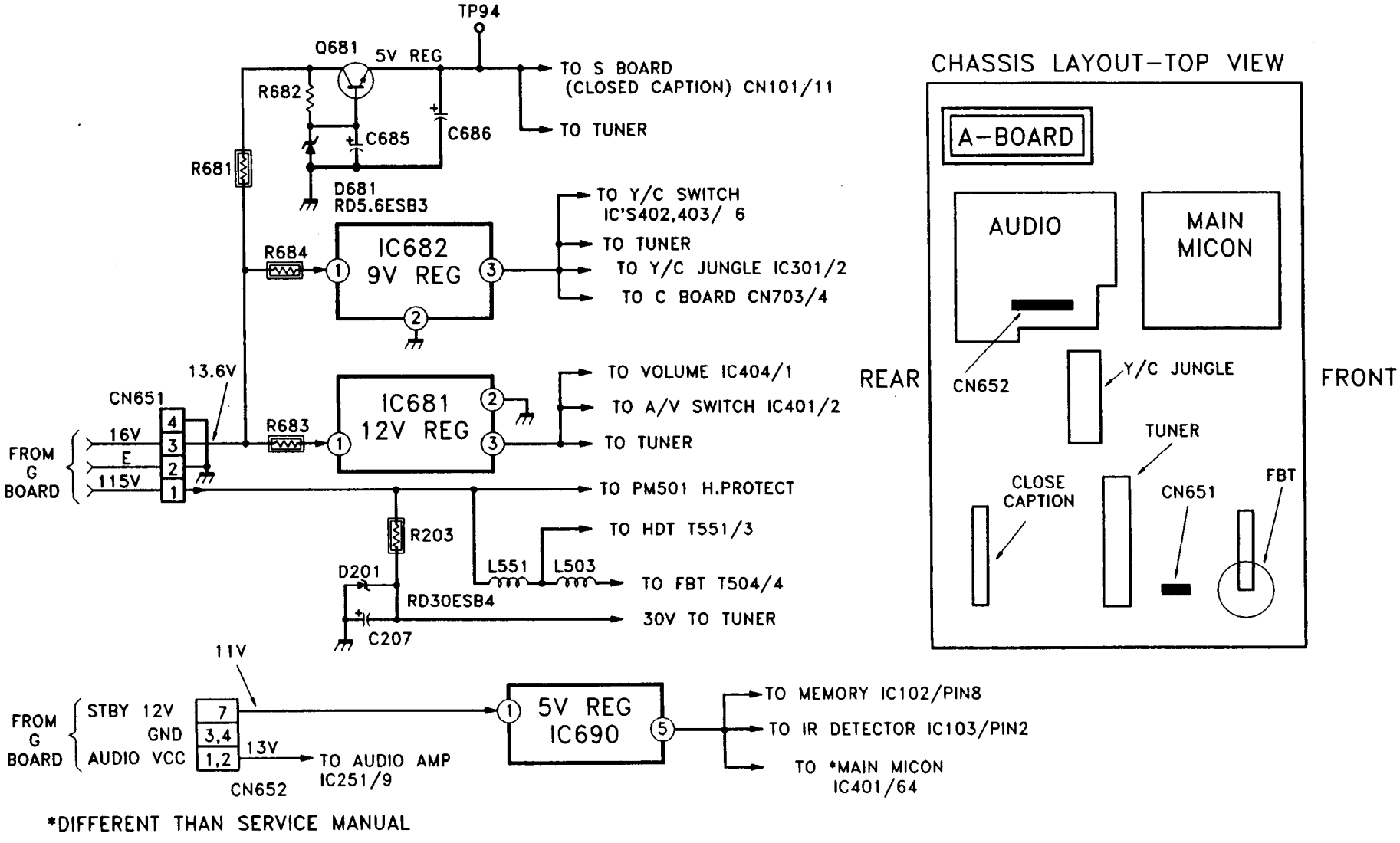
REGULATION / SOFT START

NOTES



AA-1 POWER DISTRIBUTION

NOTES



*DIFFERENT THAN SERVICE MANUAL

BA-1 POWER DISTRIBUTION

AA-1 Single Tuner Operation

The tuner in both the AA-1 and BA-1 chassis are self contained units. Although the part numbers may vary from unit to unit, the operation remains the same. Four outputs are used depending on the chassis and model number. These are video detect 1 and 2, and left and right audio. The tuner is controlled by the main micon IC101. IC101 provides the following.

- Channel selection.
- AFT (Auto Fine Tuning) control.
- Mute control.
- Switching between mono and stereo sound.

Tuner Operation Circuit Layout

The tuner circuit in the AA-1 chassis is located on three boards. The circuits are divided as follows.

1. A board contains the tuner(s).
2. UA board contains the A/V switch (see VIDEO SIGNAL FLOW for details).
3. M board contains the main micon which controls tuner operation.

Channel Set-up

When the customer turns the set ON for the first time, the memory IC102 will contain basic factory channel data. Therefore, the first thing the customer will probably do is to use the on screen menu set-up function to automatically scan and program all local TV stations. To do this, the following sequence occurs.

- Tuning data will be sent from IC101 pins 30 (data), 31 (CLK) and 22 (LATCH) to the tuner (TU101).
- The tuner will convert the data into an analog control voltage to demodulate the incoming signal. The demodulated RF is output as composite video from the tuner as VIDEO DET and VIDEO DET 2.
- The VIDEO DET output is applied to the H-SYNC detect Q001 (and associated components) which filters out the Y and C signals, and inverts the H. pulse.
- This pulse is applied to IC101 pin 28 (H - sync) where it is used to detect a valid station.
- IC101 will store the appropriate station data in the memory IC102 using the BDATN (pin 54) line and the BCLKN (pin 56) line.
- The VIDEO DET 2 output from the tuner provides composite video to the VIDEO BUFFER Q401/B for video signal processing.

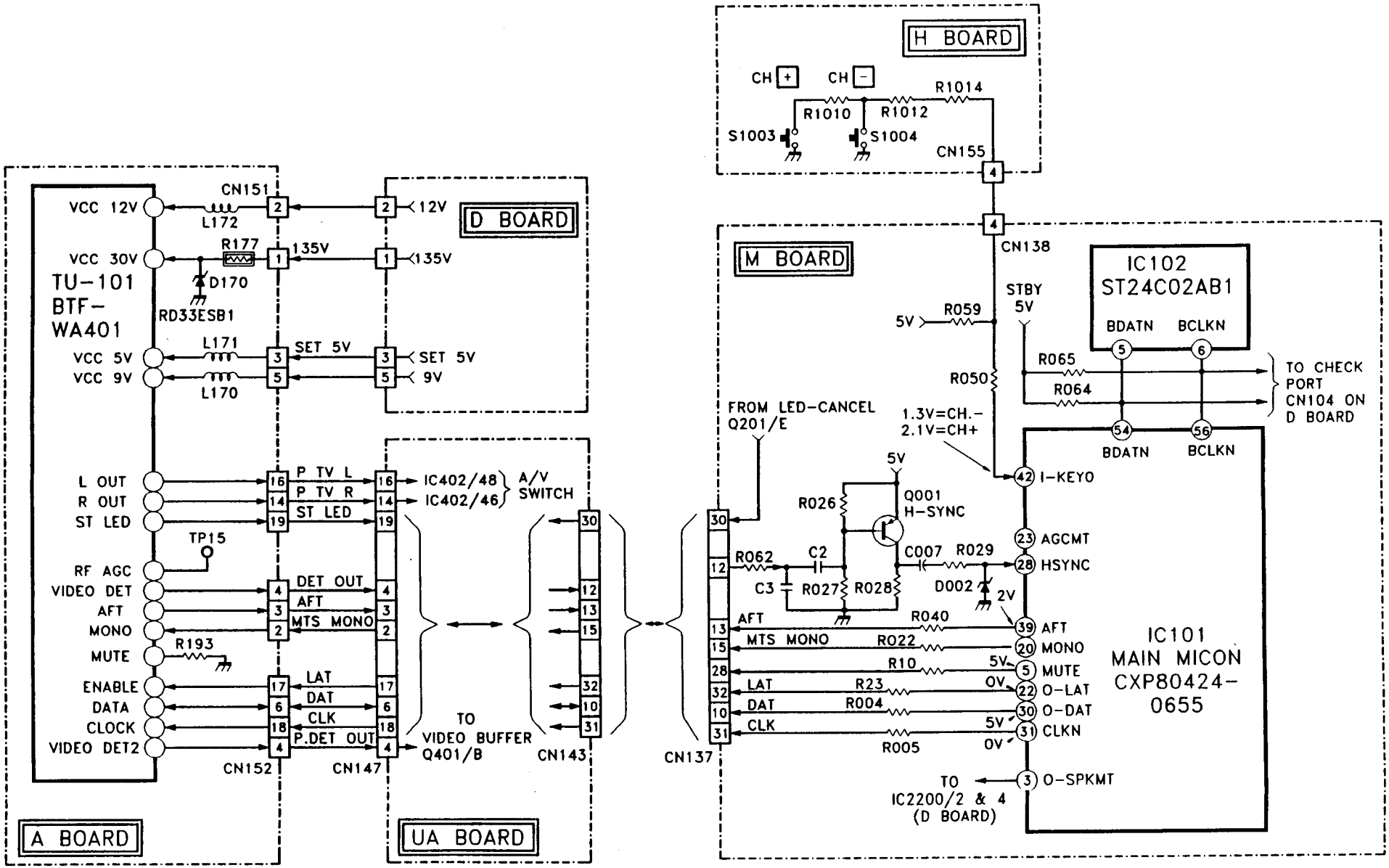
Channel Selection

Channels can be selected either by pressing a front panel channel select button (S1003 and S1004) or by pressing a select button on the remote commander. If a front panel button is used, the following voltages will be applied to IC101 pin 42 (KEY 0).

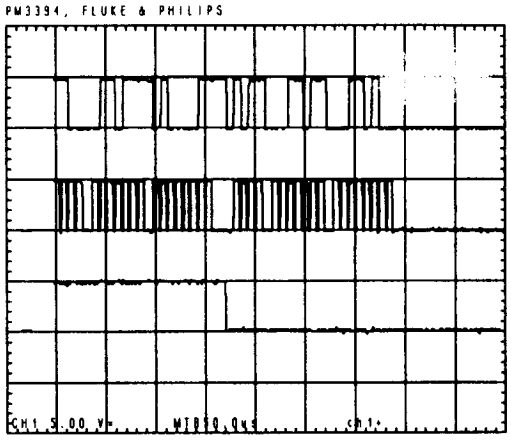
Channel UP (+) S1003 = 2.1Vdc

Channel DOWN (-) S1004 = 1.3Vdc

IC101 will then send the channel data for the appropriate channel (which had been stored in memory) to the tuner on the data, clock and latch lines. The data will take the form of a repetitive data packet at 60Hz. The waveforms shown in the schematic below show this data during normal operation. These three signals are always present.

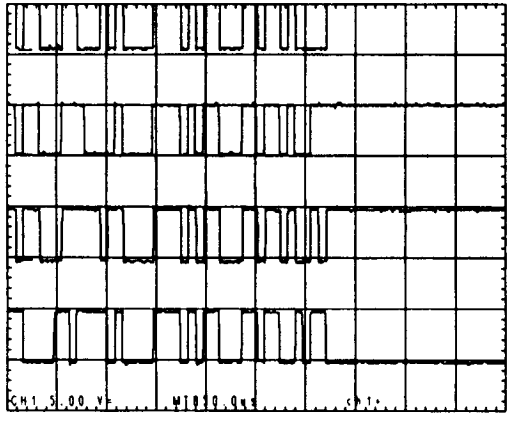


AA-1 SINGLE TUNER OPERATION



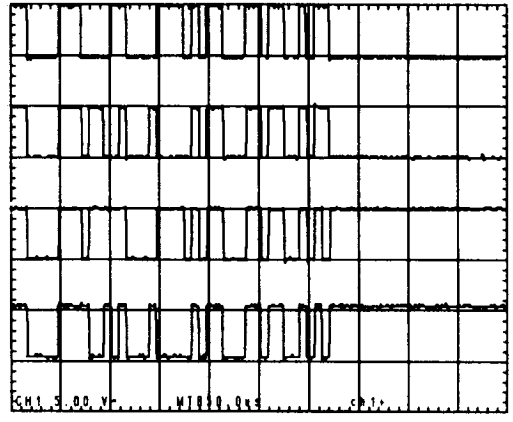
TOP IC101 pin 30 (DATA)
MIDDLE IC101 pin 31 (CLK)
BOTTOM IC101 pin 22 (LATCH)
5V/DIV. TB 50μSEC/DIV.

FIG. 1



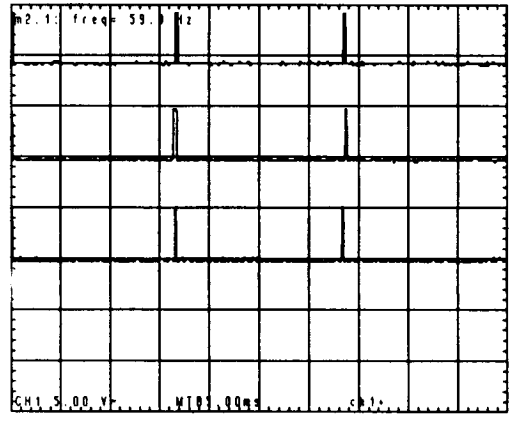
TOP IC101 pin 30 (DATA)
MIDDLE IC101 pin 31 (CLK)
BOTTOM IC101 pin 22 (LATCH)
5V/DIV. TB 50μSEC/DIV.

FIG. 3



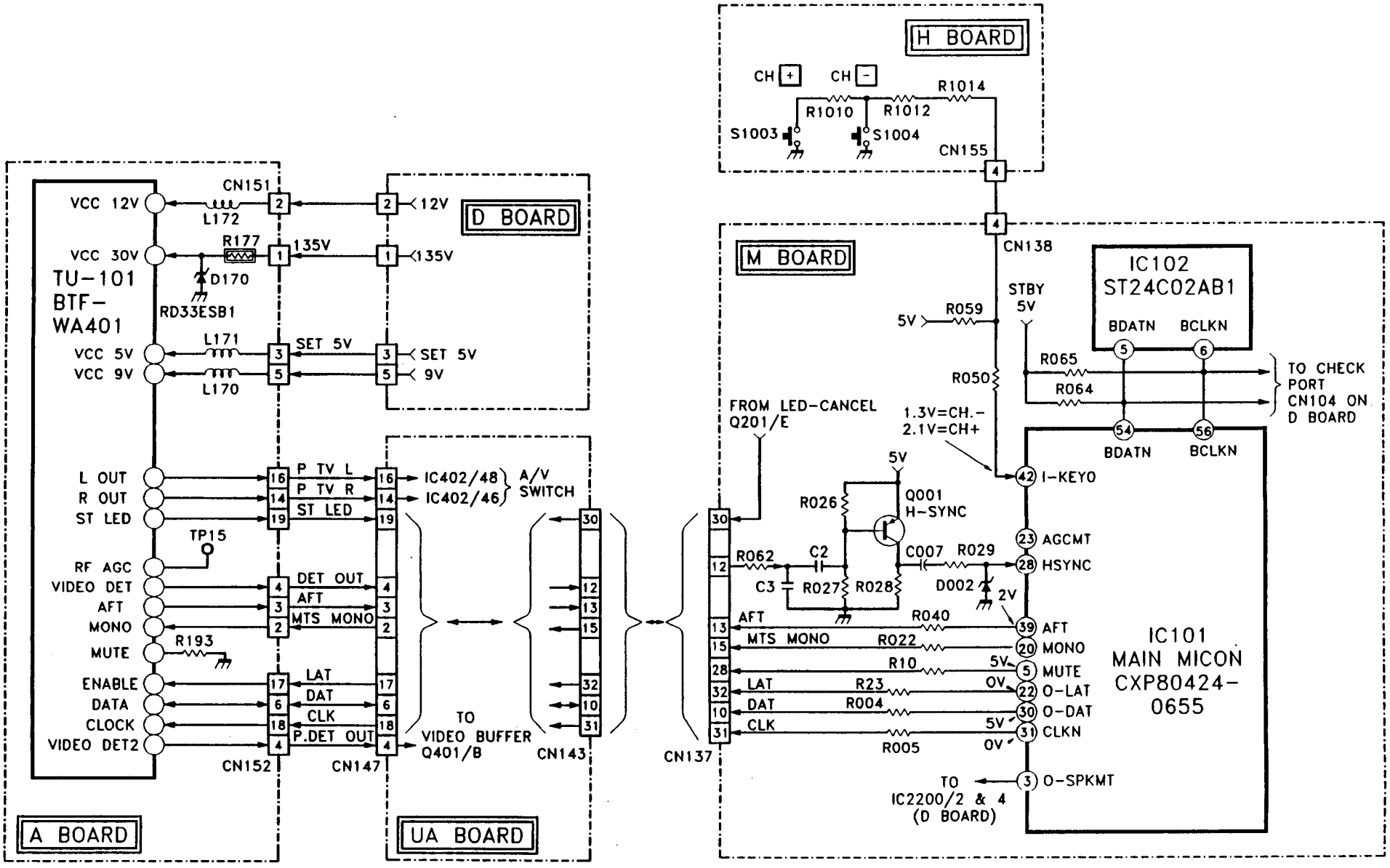
IC101 pin 30 (DATA) for TV tuner channels 2, 4, 6 and 7 (from top to bottom).
5V/DIV. TB 50μSEC/DIV.

FIG. 2



IC101 pin 30 (DATA) for TV tuner channels 2, 4, 6 and 7 (from top to bottom).
5V/DIV. TB 50μSEC/DIV.

FIG. 4



AA-1 SINGLE TUNER OPERATION

Troubleshooting

Referring to the figures on page 32 figure 1 shows the data in relation to the clock and latch lines. When the latch line is HIGH, the channel data is being sent to the tuner. If you look at figures 2 and 3, you will notice that the data is different for each channel. With this in mind, you can easily isolate a defective tuner from a defective controller. To do this simply advance channels while observing the data clock and latch lines. To observe these lines easily, set your scope as follows:

Vertical Attenuator: 5V/div.
Time base: 50usec/div.
Triggering: Negative edge/TV field

If the data continually changes but the channels do not, the tuner is probably at fault. If the data remains the same or the clock line and latch lines are intermittent, the controller is probably at fault.

Figure 4 shows the same three signals at a time base of 5msec/div. so that you can verify that the repetitive data packet is at 60Hz.

AFT Control

The AFT signal is a varying dc feedback voltage which tells the tuner control IC101 what the RF level is. IC101 will change the tuning voltage until the maximum RF level is achieved. This will take place with or without an H pulse present although a station will be tuned alot quicker with the H pulse present. The nominal AFT voltage is 2.1Vdc.

Mute Control

The main micon will mute the audio signal under two conditions.

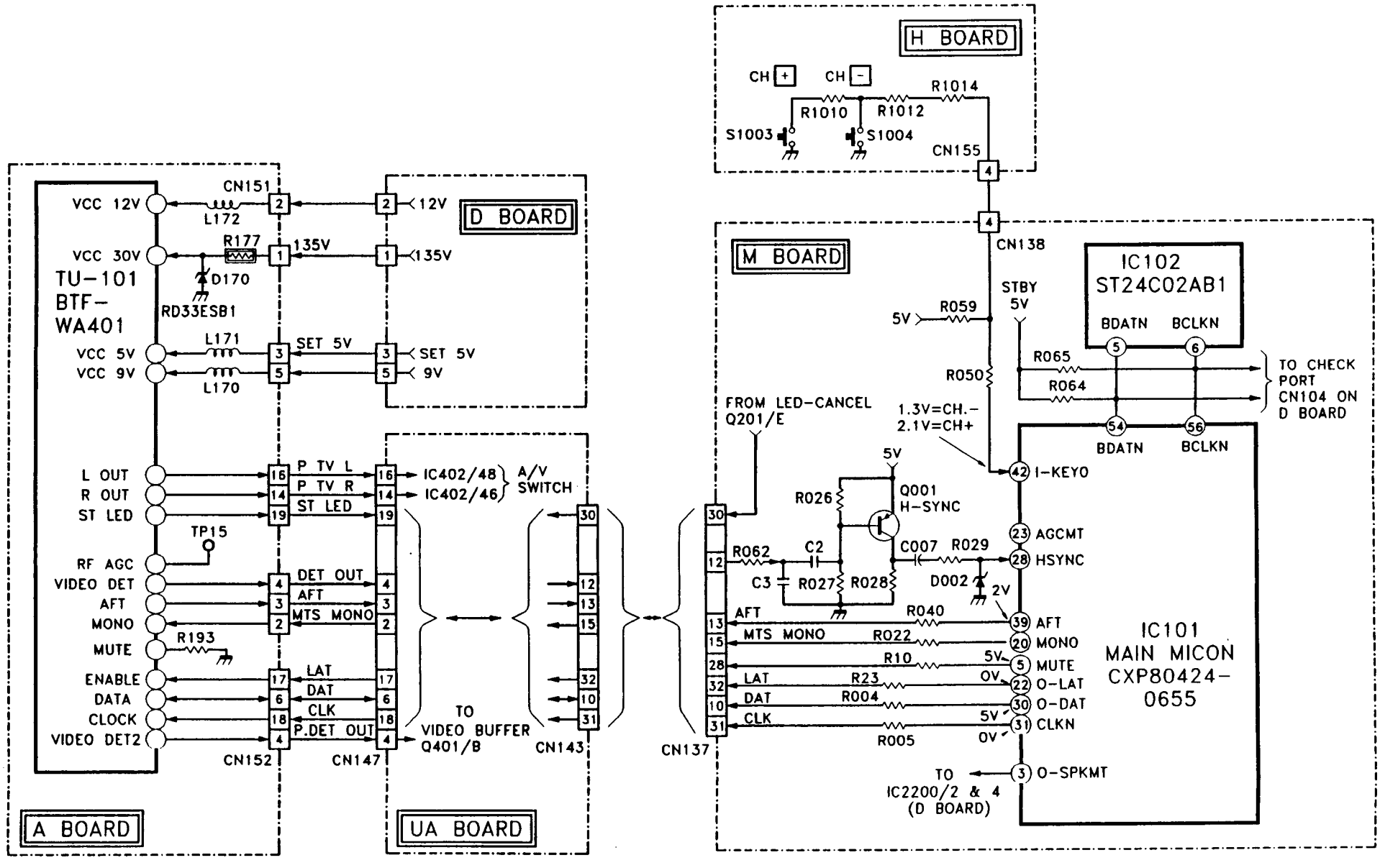
- Between stations
- When the MUTE button on the remote commander is pressed.

To mute the audio between stations, data from the main micon IC101 pin 30 (O-DAT) is used.

When the MUTE button on the remote commander is pressed, IC101 pin 3 (SPKMT) will go HIGH. This is applied to the mute circuitry for the audio amp only on the D board (not shown - refer to the AUDIO PROCESS section).

Switching Between Mono and Stereo

The customer can manually switch between mono and stereo operation using the on screen menus. When mono is selected, IC101 pin 20 will go HIGH. In all other modes, this pin will be LOW.



AA-1 SINGLE TUNER OPERATION

AA-1 Video Signal Flow / Switching

The AA-1 chassis has the option of containing two tuners and a PIP (picture in picture) circuitry. Those sets which contain two tuners (KV-32TS46) can have two TV programs appear on the screen at the same time. All other sets will only allow one TV program to be viewed at one time. If the PIP function is selected on these sets, the main tuner output will be seen as the main picture as well as the child picture. The circuit description that follows applies to the following models; KV27TS36, KV32TS36 and KV32TS46. For all other models, refer to the A/V switching section.

Circuit Description of Main Tuner Signal Flow

The main tuner video signal (P DET OUT) is buffered by Q402 and applied to the Video switch IC402 pin 47. This signal is amplified to and is output at pin 40. This composite video signal is applied to a comb filter which separates the signal into Y and C components. The BA-1 chassis however does not contain a comb filter instead, discrete filtering is used at the input of the Y/C jungle. The output of the comb filter is applied back to the video switch at pins 37 (Y IN 1) and 35 (C IN 1). The Y and C outputs of the video switch (pins 43 and 45) can be switched between TV video (or VID 1, 2 or 3) and S-video which is applied to pins 31 (Y) and 5 (C). Switching is accomplished via data from the main micon, on the I^2C bus. This will be explained later.

The Y and C outputs are buffered by Q405 (Y) and Q406 (C) and applied to the PIP processor on the P board. The video signal is processed on this board even if the PIP function is not selected. Therefore, if there is a problem with the quality of the picture or lack of picture, The problem may be on the PIP board. These problems can be mistaken for defects in other areas such as the IK lines, muting circuits, Y/C jungle or RGB drives. Before you troubleshoot these areas, make sure that the video signal is present at the input of the Y/C jungle IC301 pins 3 and 5 (M board). If it is not, you can bypass the PIP board as follows:

1. Locate the P board connector CN150.

2. Jumper pin 1 (C OUT) to pin 5 (C IN) and pin 3 (Y OUT) to pin 7 (Y IN).

This will bypass the P board so that the Y and C signals are applied directly to the Y/C jungle. PIP processing will be explained in the PIP section of the manual.

After being processed by the PIP processor, the Y and C signals are applied to the Y/C jungle IC301 pins 3 (Y) and 5 (C). In addition, the Y signal is also applied to the closed caption IC150 pin 11 (V IN). The Y/C jungle mixes the video signal, the closed caption signal, and the on screen display information from the main micon and outputs the composite signal as RGB at pins 20 (R), 22 (G) and 24 (B). The RGB outputs are then applied to the C board to be amplified by the video amps.

S-Video Switching

When the S-VIDEO cable is connected, the switch output in the connector will be grounded. This signal is connected to both the A/V switch IC402 pin 6 (SIN1) and the main micon IC101 pin 9 (SSWN). As a result, the following will occur:

1. A/V switch will automatically switch to the S-VIDEO input at pins 3 and 5.

2. The main micon will change the on screen menu to show that the S-Video input had been connected.

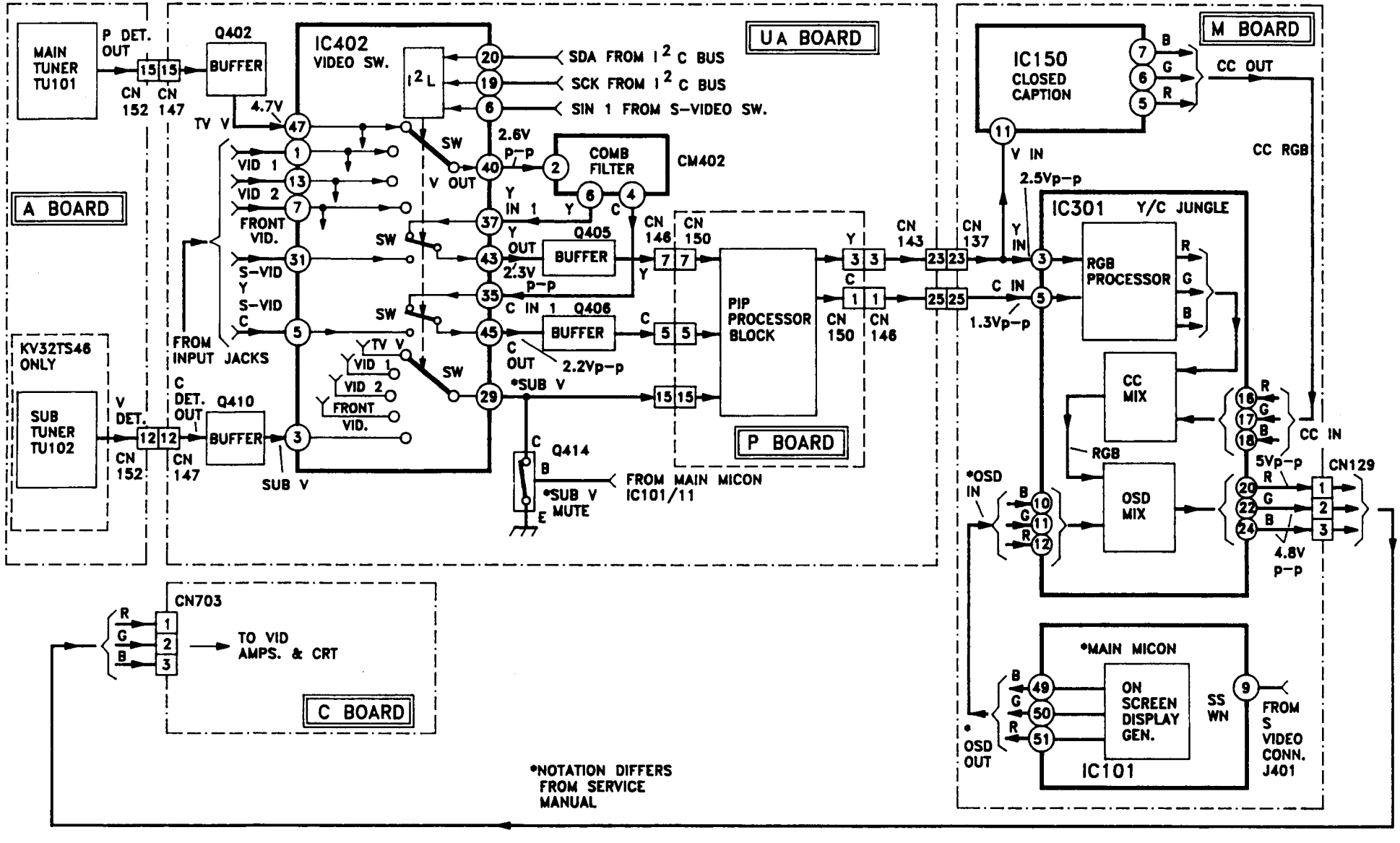
As long as the S-VIDEO connector is in place, the VIDEO 1 input cannot be used since the S-VIDEO signal has priority. Also, the on screen display will not show that the S-VIDEO input is being displayed. It will continue to display VIDEO 1.

Sub Tuner Signal Switching

The sub tuner is only available on the KV32TS46. When PIP is selected, the sub tuner signal will be output from the A/V switch at pin 29 and applied directly to the PIP processor. There is no comb filter used for the child picture in this set. Instead, a discrete filter located on the P board is used to separate the Y and C components. On units with a single tuner, Q414 is used to mute the sub V line to prevent noise.

Video Signal Switching in PIP Mode

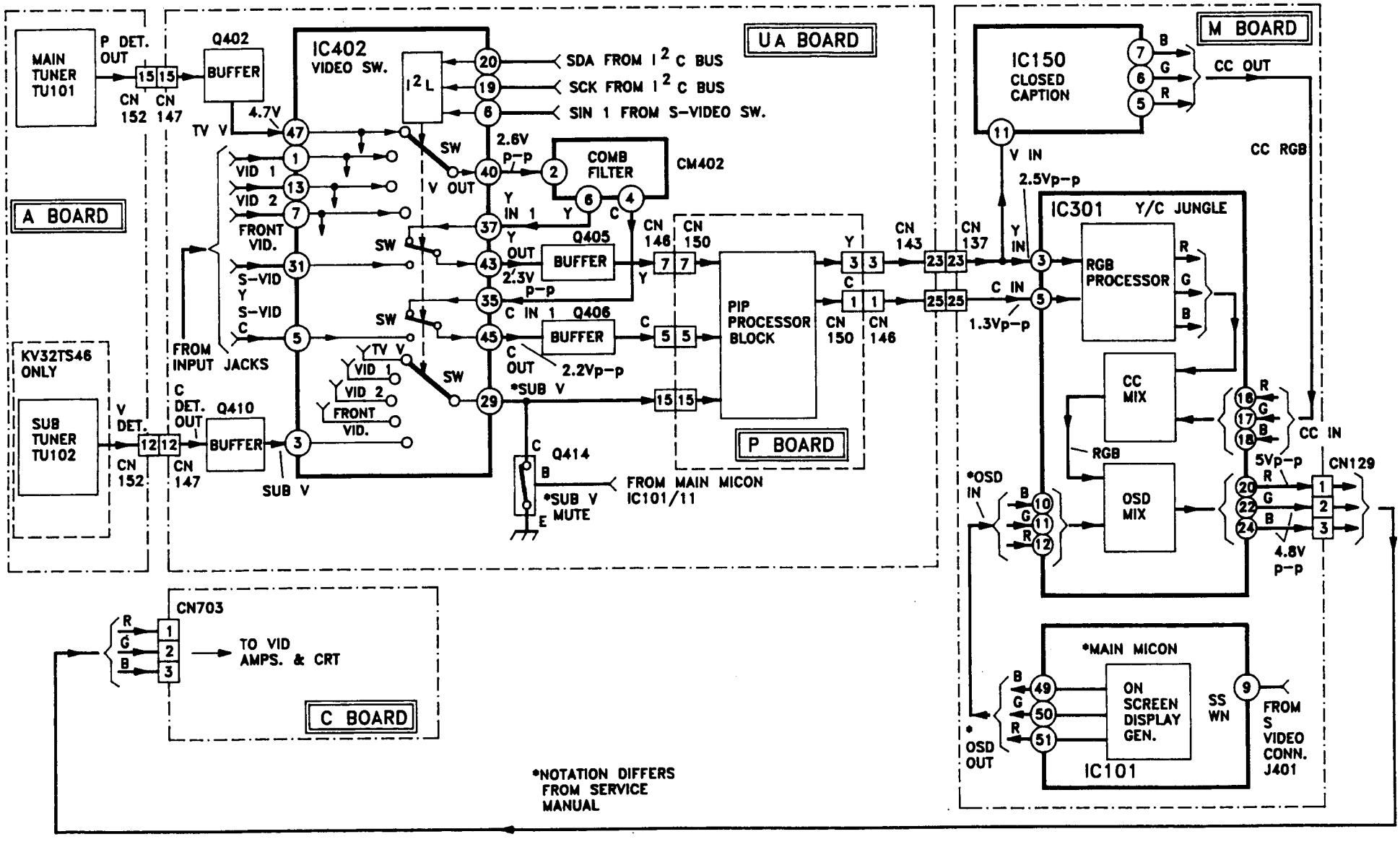
The A/V switch is set up so that all video inputs are available at both the VOUT (pin 40) and the SUB V (pin 29). When the user selects a source for the main picture and the child picture, the video switch will receive the data



AA-1 VIDEO SIGNAL FLOW / SWITCHING

at pin 20 (SDA) and respond by switching each output to the appropriate source.

NOTE: If there is no main picture, the child picture will not be in color. Also, If you select TV while in PIP mode, the main picture and the child picture will be the same in single tuner sets.



AA-1 VIDEO SIGNAL FLOW / SWITCHING

BA-1 Single Tuner Operation

The tuner in BA-1 chassis is a self contained RF, VIF and audio unit. Although the part number may vary from unit to unit, the operation remains the same. The tuner, BTF-WA401, has three outputs: video, left and right audio. The BTF-LA401 tuner is basically used as the sub tuner to provide the PIP picture in the dual tuner AA-1 chassis sets and to provide the mono only audio in the 13 inch BA-1 chassis sets. Both tuners are controlled by the Main Micon IC101. IC101 provides the following:

- Channel selection
- AFT (Auto Fine Tuning) control
- Mute control
- Switching between mono and stereo sound (BTF-WA401 tuner)

Channel Set-up

When the customer turns the set on for the first time, the memory IC102 will not contain any channel data. Therefore, the first thing the customer will probably do is use the on screen menu to automatically scan the incoming RF and program all local stations. To do this, the following sequence occurs.

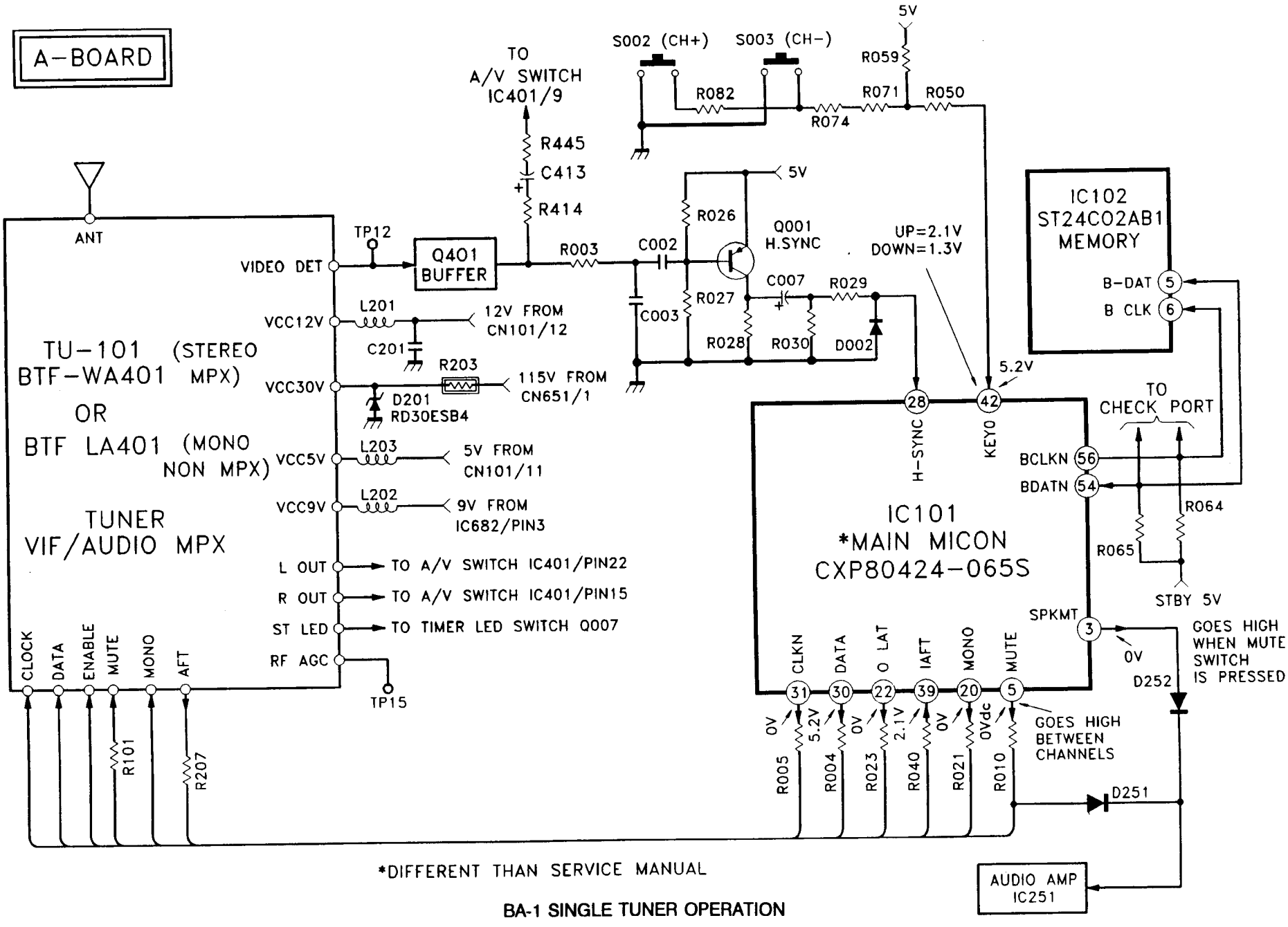
- Tuning data will be sent from IC101 pins 30 (data), 31 (CLK) and 22 (LATCH) to the tuner (TU101).
- The tuner will convert the data into an analog control voltage to tune the incoming signal. The demodulated RF is output as composite video from the tuner as VIDEO DET.
- The composite video signal is buffered by Q401 (not shown) and applied to a H. sync detector Q101 (and associated components) which filters out the Y and C signals, and inverts the H. pulse.
- This pulse is applied to IC101 pin 28 (H sync) where it is used to detect a valid station.
- IC101 will store the appropriate station data in the memory IC102 using the BDATN (pin 54) line and the BCLKN (pin 56) line channel selection.

Channels can be selected either by pressing a front panel channel select button (S003 and S002) or by pressing a select button on the remote commander. If a front panel button is used, the following voltages will be applied to IC101 pin 42 (KEY 0).

Channel UP (+) S002 = 2.1Vdc

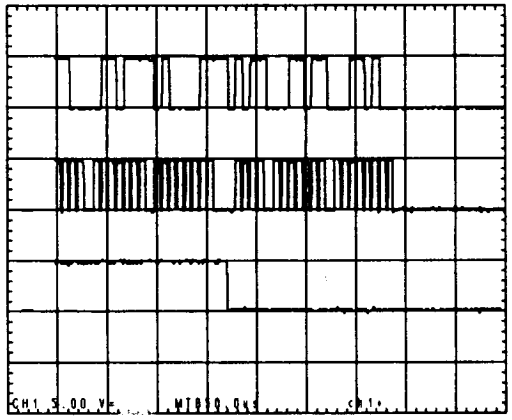
Channel DOWN (-) S003 = 1.3Vdc

IC101 will then send the channel data for the appropriate channel (which had been stored in memory) to the tuner on the data, clock and latch lines. The data will take the form of a repetitive data packet at 60Hz. The waveforms shown in the schematic below show this data during normal operation. These three signals are always present.



*DIFFERENT THAN SERVICE MANUAL

BA-1 SINGLE TUNER OPERATION

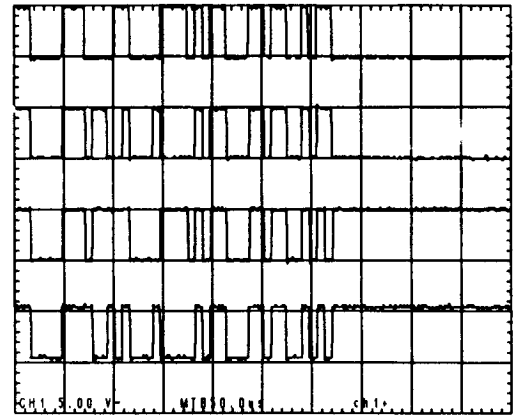


TOP IC101 pin 30 (DATA)
MIDDLE IC101 pin 31 (CLK)
BOTTOM IC101 pin 22 (LATCH)
5V/DIV. TB 50μSEC/DIV.

FIG. 1

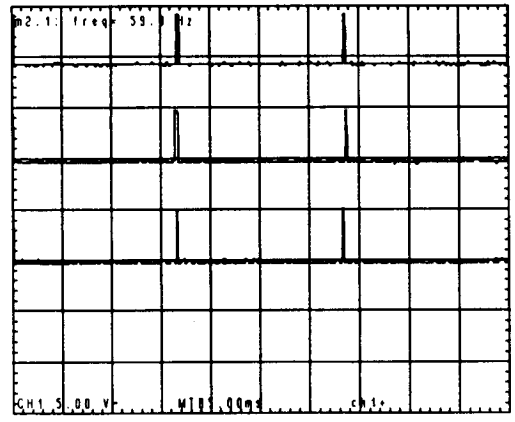
IC101 pin 30 (DATA) for TV tuner channels 2, 4, 6 and 7 (from top to bottom).
5V/DIV. TB 50μSEC/DIV.

FIG. 2



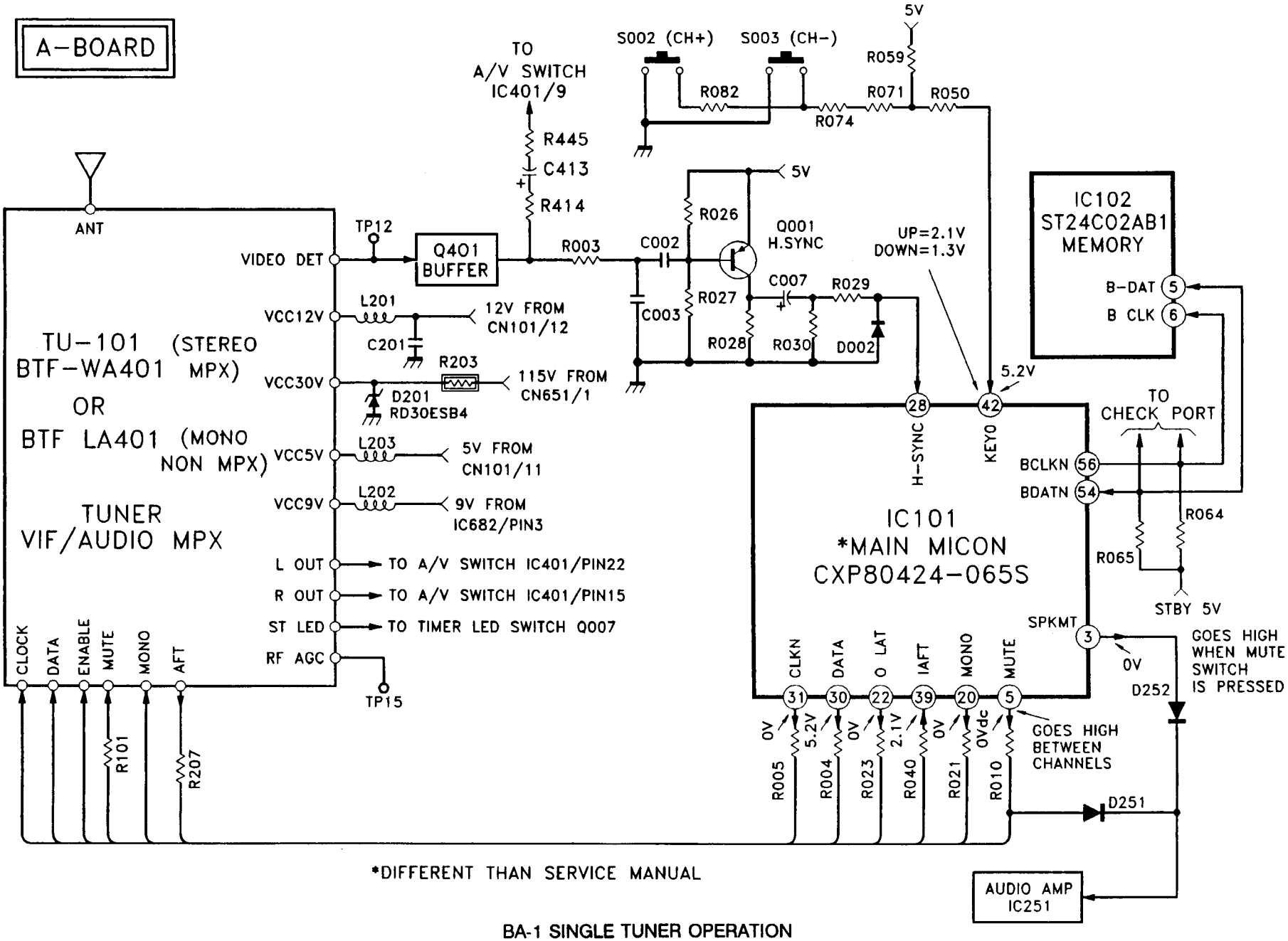
IC101 pin 30 (DATA) for TV tuner channels 2, 4, 6 and 7 (from top to bottom).
5V/DIV. TB 50μSEC/DIV.

FIG. 3



TOP IC101 pin 30 (DATA)
MIDDLE IC101 pin 31 (CLK)
BOTTOM IC101 pin 22 (LATCH)
5V/DIV. TB 50μSEC/DIV.

FIG. 4



*DIFFERENT THAN SERVICE MANUAL

BA-1 SINGLE TUNER OPERATION

Troubleshooting

Referring to the figures on page 42 figure 1 shows the data in relation to the clock and latch lines. When the latch line is HIGH, the channel data is being sent to the tuner. If you look at figures 2 and 3, you will notice that the data is different for each channel. With this in mind, you can easily isolate a defective tuner from a defective controller. To do this simply advance channels while observing the data clock and latch lines. To observe these lines easily, set your scope as follows:

Vertical Attenuator: 5V/div.

Time base: 50usec/div.

Triggering: Negative edge/TV field.

If the data continually changes but the channels do not, the tuner is probably at fault. If the data remains the same or the clock line and latch lines are intermittent, the controller is probably at fault.

Figure 4 shows the same three signals at a time base of 5msec/div so that you can verify that the repetitive data packet is at 60Hz.

AFT Control

The AFT signal is a varying dc feedback voltage which tells the tuner control, IC101, what the IF center frequency is. IC101 will change the tuning voltage until the maximum IF level is achieved. This will take place with or without an H pulse present although a station will be tuned alot quicker with the H pulse present. The nominal AFT voltage is 2.1Vdc.

Mute Control

The tuner control will mute the audio signal under two conditions.

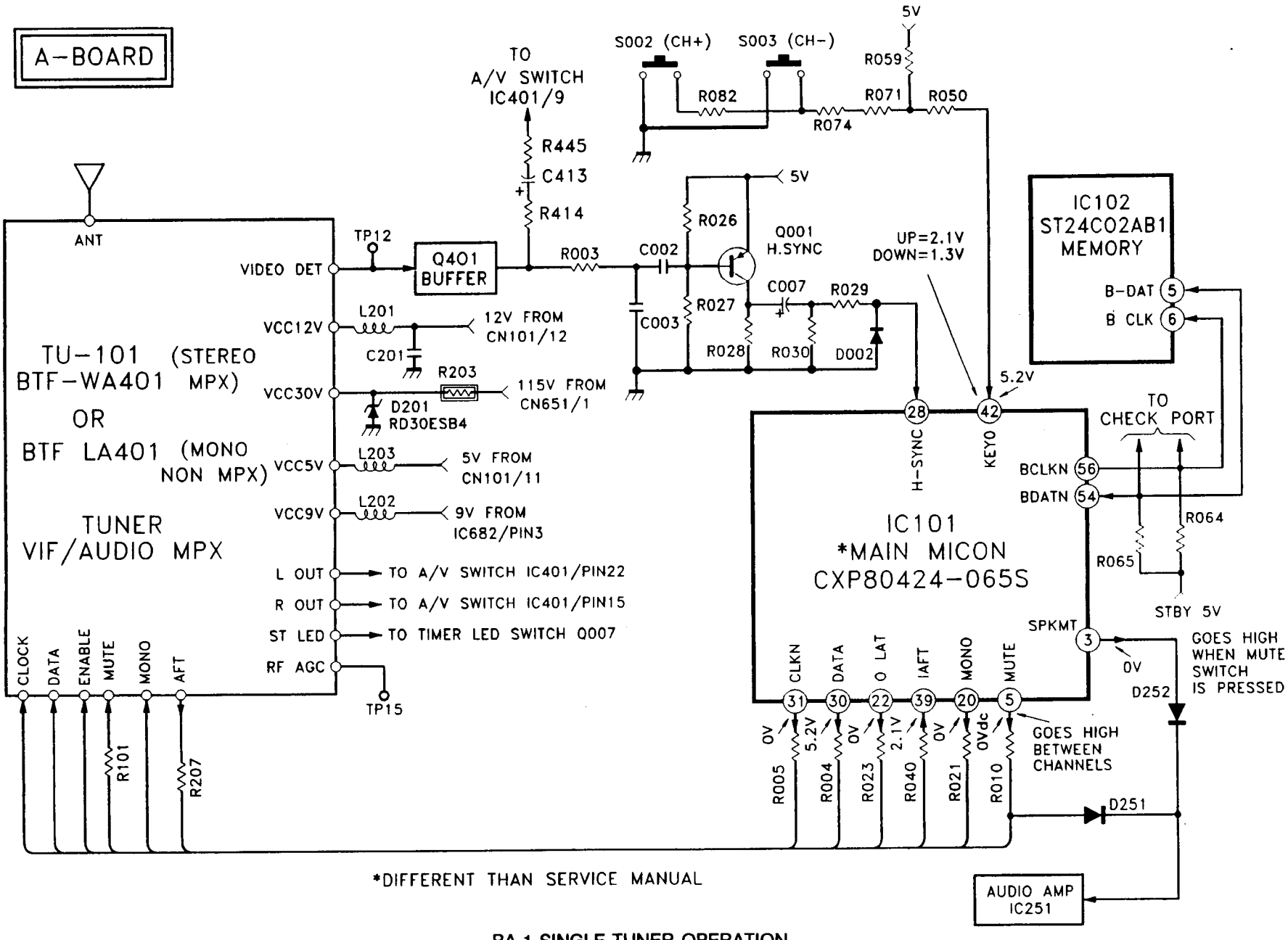
- Between stations
- When the MUTE button on the remote commander is pressed.

To mute the audio between stations, IC101 pin 5 (MUTE) will go HIGH. This signal is applied to the tuner and to the audio amp IC251 (through D251).

When the MUTE button on the remote commander is pressed, IC101 pin 3 (SPKMT) will go HIGH. This is applied to the audio amp only (through D252).

Switching Between Mono and Stereo

The customer can manually switch between mono and stereo operation using the on screen menus. When mono is selected, IC101 pin 20 will go HIGH. In all other modes, this pin will be LOW.



*DIFFERENT THAN SERVICE MANUAL

BA-1 SINGLE TUNER OPERATION

BA-1 A/V Switching

The BA-1 chassis has four inputs as shown below. These are: Antenna, Video 1, Video 2 and S-Video. These signals are switched by the A/V switch, IC401, the Y switch, IC402, and the C switch, IC403. The tuner (antenna) and video 2 can be selected at any time. Video 1 can only be selected if the S video input (J401) is disconnected. Otherwise, the S video input has priority. These three switches are controlled by the main micon, IC101, through three control lines from IC101 pin 6 (V0), pin 7 (V1) and pin 8 (V2). The switching circuit operates as follows.

Selecting an Input

Inputs are selected by either pressing the front panel TV/VIDEO switch S006, or by using the remote commander (not shown). Each time the TV/VIDEO switch is pressed, IC101 pin 42 will go to 2.5Vdc. This also causes the on screen graphics for the input selected to be displayed on the CRT temporarily.

Switching Between Inputs

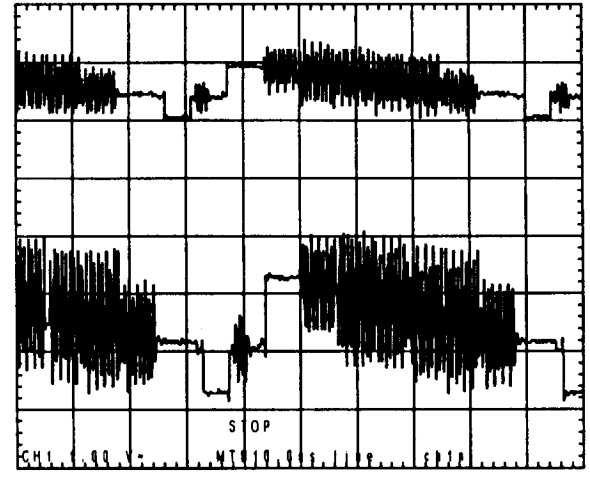
The A/V switch IC401 is used to select between the tuner, VIDEO 1, J402 (rear panel) and, J403, (front panel). To do this, two control lines at pins 4 and 6 are used. A 2-bit code is generated by IC101 pin 6 (V1) and 7 (V0) to accomplish the switching. The following chart shows the code.

	TV	VIDEO 1	VIDEO 2
IC101 pin 6	5.2Vdc	0	5.2Vdc
IC101 pin 7	5.2Vdc	5.2Vdc	0

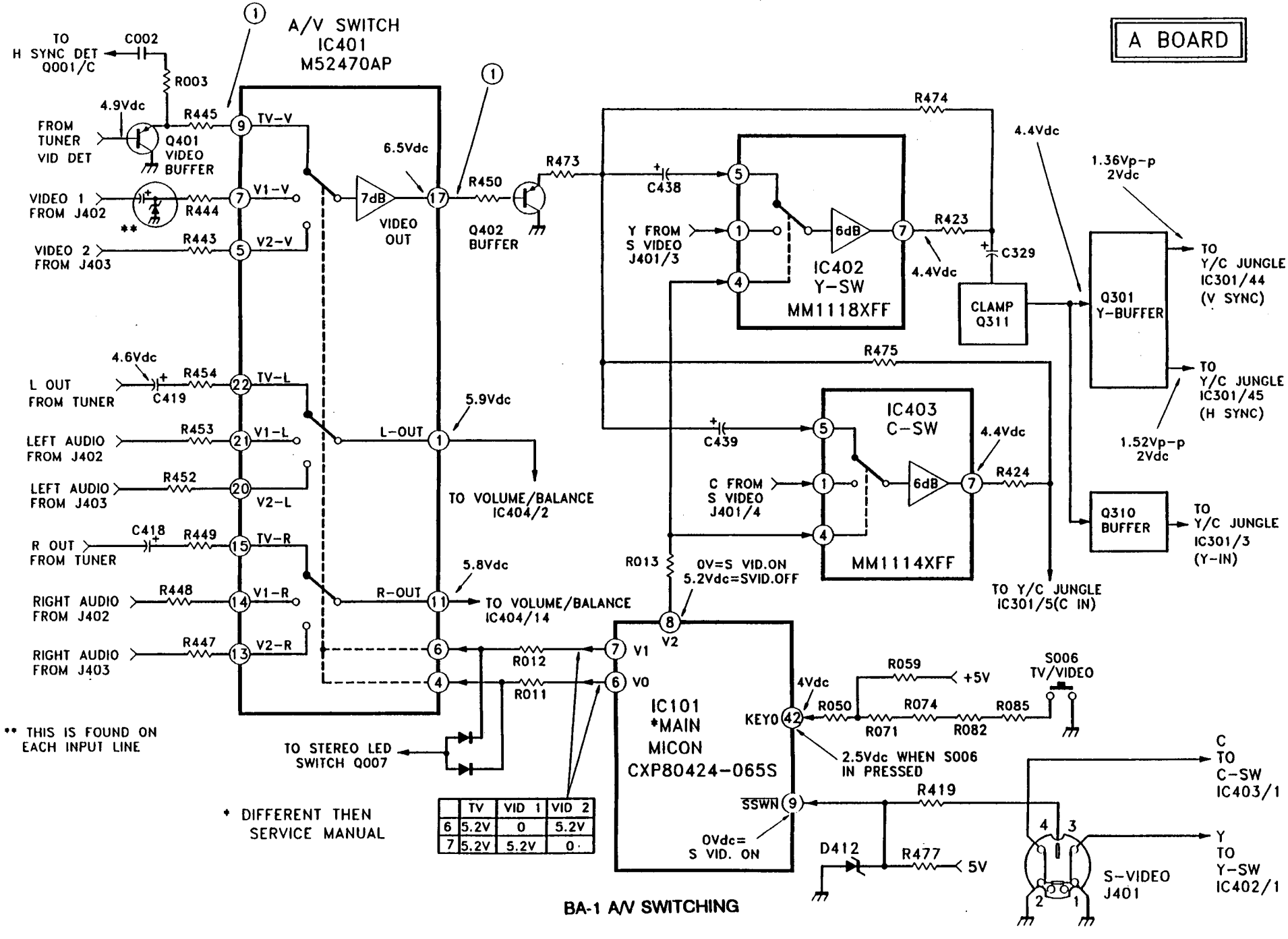
The A/V switch has three switches in it to switch the video signal, and left and right audio signals separately. The video switch has a 7dB amplifier to increase the voltage gain of the video signal from 1.4Vp-p at its input (pins 5, 7, and 9) to 3Vp-p at the output (pin 17). This is shown in the figure on the right.

The Y switch, IC402, and the C switch, IC403, are identical switches used to select between tuner video at pin 5 and either video 2 or S video at pin 1. These switches are controlled by a switching signal from IC101 pin 8 (V2). This signal will go LOW when the S video cable is plugged in and VIDEO 1 is selected. At this time, IC101 pin 9 (SSWN) will go LOW as a result of the switch in the S video connector closing. A 6dB amplifier inside both of these switches changes the 1.3Vp-p signal input to IC402 and IC403 pins 5 to a 2.7Vp-p signal at pins 7. These waveforms will look similar to the ones in the figure below.

The Y signal is clamped and buffered by Q311 and Q301 and applied to the Y/C jungle IC301 pins 45 (H sync), 44 (V sync), and pin 3 (Y-IN). The C signal is applied to the Y/C jungle IC301 pin 5 (C IN).



IC402 and IC403 pin 5 (Top)
IC402 and IC403 pin 7 (Bottom)



BA-1 A/V SWITCHING

AA-1 Audio Process

The Audio circuitry in the AA-1 chassis is located on four boards. The circuits are divided as follows:

1. A board contains the tuner and the speaker connections.
2. UA board contains the A/V switching and I/O jacks to select input sources
3. M board contains the audio processor and variable audio amp for volume, bass, treble and balance adjustment.
4. D board contains the muting circuit and the audio power amp.

A/V Switching

All audio sources enter the UA board and are applied to the A/V switch IC402 through a series resistor and capacitor. The number of inputs depends upon the particular model. The switching of signals is performed by the switch from a command by the main micon. The command is applied to the switch on the I^2C bus. The audio signals will the exit the switch from two outputs at pins 26 (left) and 28 (right). The A/V switch uses only two outputs for audio although the switch has provisions for 6 outputs. The outputs of the A/V switch are coupled through C413 and C416 to the audio processor IC201 on the M board.

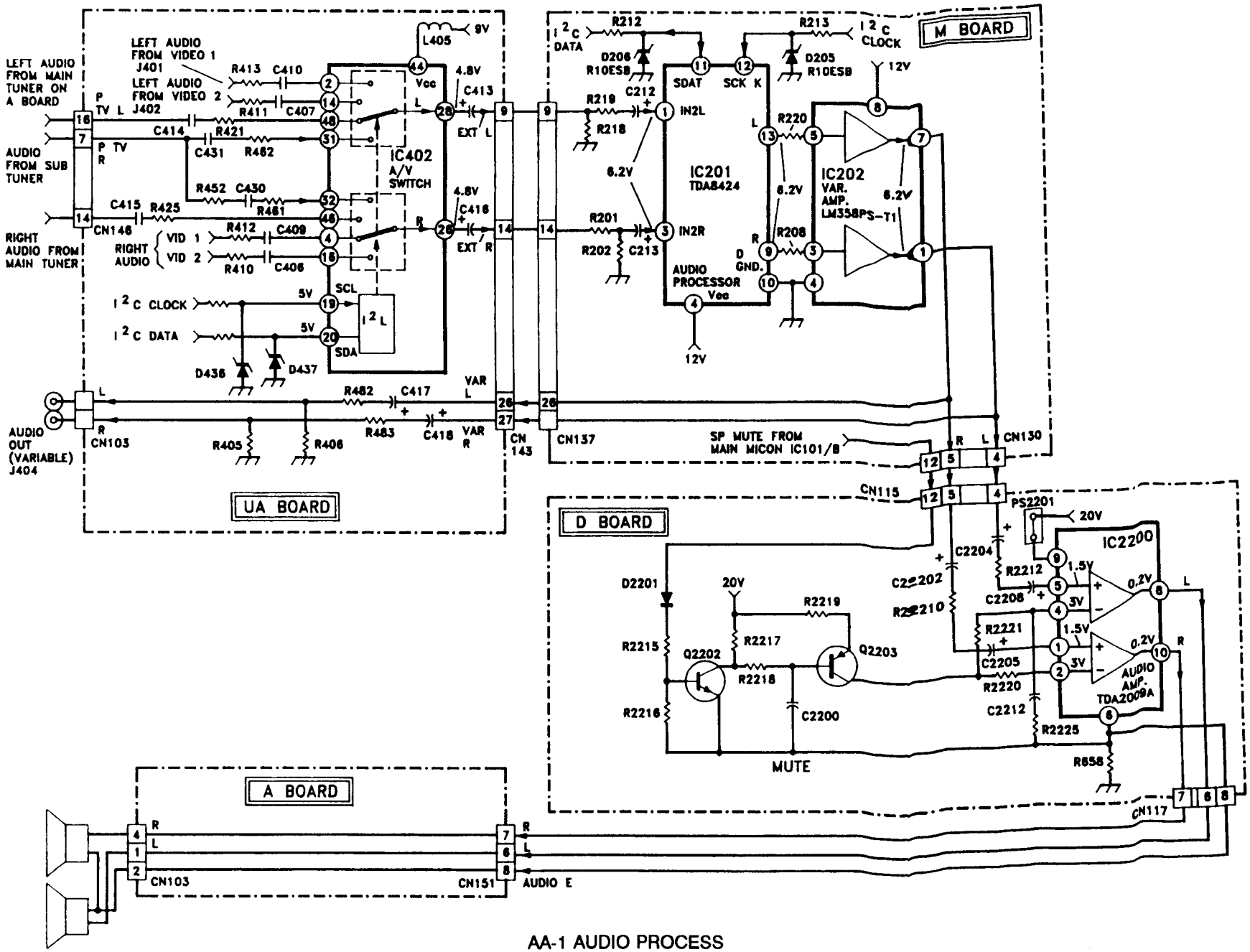
Audio Processor

The audio processor in this chassis uses data from the I^2C bus to adjust the audio parameters such as volume, bass, treble and balance. Once processed, the audio signals are output from IC201 pins 13 (left) and 9 (right) and applied to a fixed gain amplifier IC202 through R220 (left) and R208 (right). IC202 provides a gain of 2 so that a 50mv input signal will be output at 100mv. The amplified audio signals are then applied to the audio amp IC2200 on the D board.

Audio Amplifier

The audio amplifier provides power gain [illegible] and right audio signals. Each signal is coupled through a series resistor and capacitor to the non-inverting inputs of the amplifier IC2200 pins 5 (left) and 1 (right). A muting circuit composed of Q2202 and Q2203 is [illegible] to the inverting inputs of the amplifier IC220 pins 4 (left) and 2 (right) through series resistors R2221 (Left) and R2220 (right). When the mute button on the remote commander is pressed, main micon IC101 pin 3 (SP MUTE) will go HIGH. As a result, a mute switch Q2202 will be turned on through D2201. Q2202 will turn ON mute switch Q2203 which brings the inverting inputs of amplifier IC2200 up to 3.6Vdc. Acting as a comparator, the amplifier will not pass the audio signal since the bias on the inverting inputs is much higher than that of the non inverting inputs.

The outputs of the audio amplifier IC2200 pins 8 (left) and 10 (right) are applied to one side of each speaker connected to the A board. The ground return for both speakers float above chassis ground through R658. Notice that all the audio amplifier IC2200 circuitry also floats above chassis ground through R658.



AA-1 AUDIO PROCESS

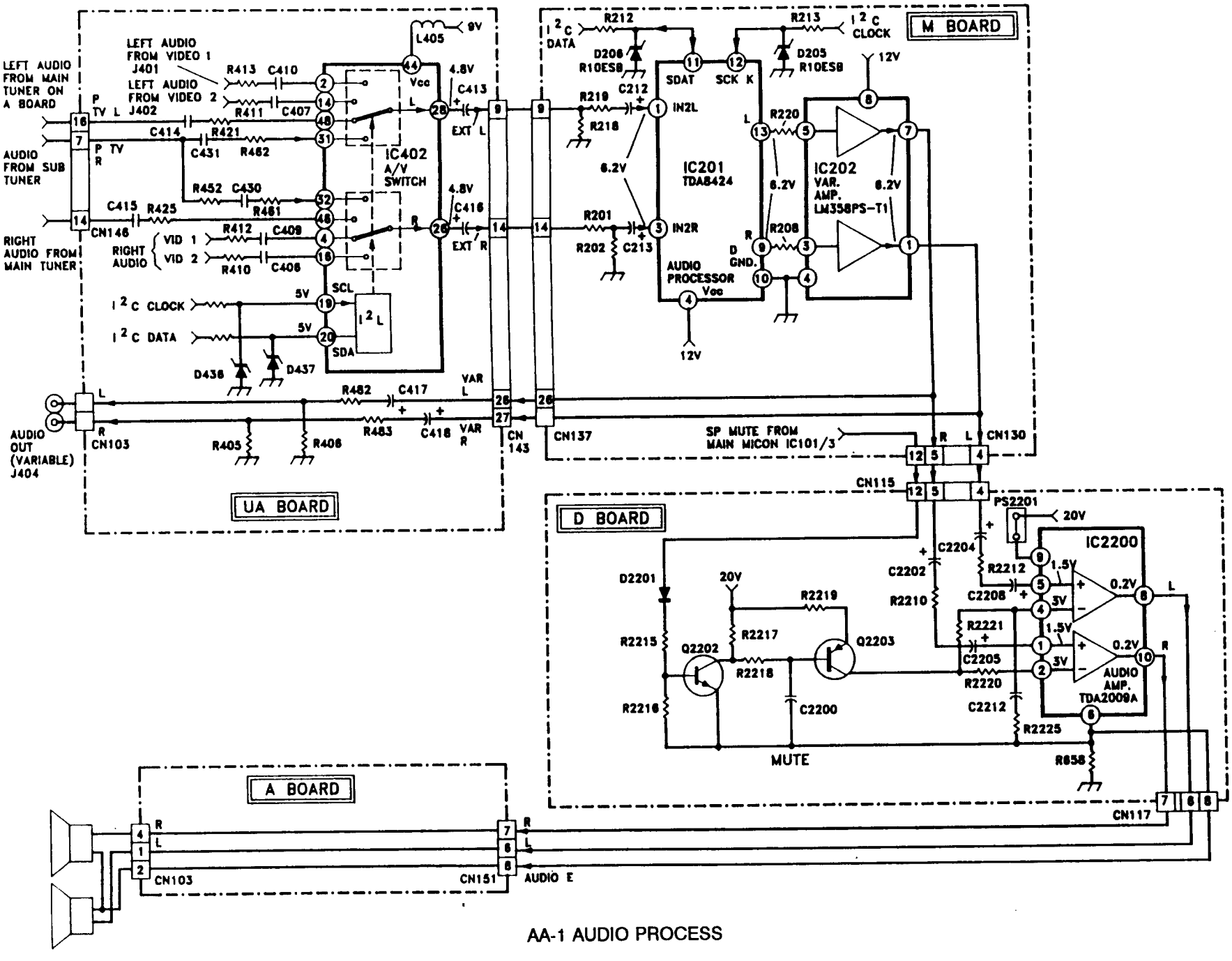
Troubleshooting

The first step in troubleshooting the audio process circuitry is to check the must-haves. In this case, the must-haves are:

1. Power for each IC on each board as follows.
   - 9V on the A board.
   - 12V on the M board.
   - 20V on the D board and fuse PS2201.
2. Check for proper data and clock signals on the I^2C bus at IC201 pins 11 (data) and 12 (clock).

If the above items check out ok, make sure that the muting circuit is not operating. To do this verify that IC2200 pins 2 and 4 are at a 3V level or below. If not, troubleshoot the mute circuit. Then check to see that the A/V switch is passing the audio signal by signal tracing through it. If there is a question regarding the A/V switch, jumper the input and output pins to bypass it.

To signal trace the audio process circuit, input a 1kHz 500mV sinewave at any video input and trace it through.



AA-1 AUDIO PROCESS

Super Woofer

A super woofer is a single channel low frequency reinforcement device. It is used to add extra bass to small speaker systems which cannot produce enough bass due to their small size. Since very low frequencies are non directional, the left and right audio signals are mixed together to produce one channel. The SA-W200 active super woofer is an accessory provided with the KV32TS46. It is a self contained unit equipped with its own power supply and automatic internal power switch.

Circuit Description

The super woofer circuitry is divided into four sections; mixing, filtering, amplification and switching. For testing purposes, a 0.775Vp-p 100Hz sine wave was applied to the unit. The peak to peak voltages which appear in the diagram below are a result of that input signal.

Mixing

Left and right audio signals from the variable output of the tv set are coupled to buffer IC001 pins 6 (left) and 4 through C003 (left) and C004. The 40mVp-p output of the buffer is applied to the inverting input of mixer IC002 pin 7. The mixer adds the left and right channels together as well as providing some gain to the signal. The 60mVp-p signal is then applied to the 1st filter stage.

Filtering

The output of the mixer is applied to the low pass filter IC003 pin 4. Two stages of filtering provide an 18dB/octave roll-off low pass filter. At the tested frequency, the 20mVp-p input signal at IC003 pin 4 was reduced to 10mVp-p at pin 8. The output of the second stage at pin 8 is coupled by C009 to variable resistor VR001. VR001 is a volume control which is mounted in the front case.

The following list is provided to aid in troubleshooting.

FREQ.	VOLTAGE AT SPEAKER
50HZ	1.5Vp-p
100HZ	300mVp-p
200HZ	50mVp-p

Amplification

The woofer signal from VR001 is coupled by C010 and applied to the amplifier IC005. IC005 then provides a push-pull type signal to the woofer SP901. The two outputs from pins 11 and 16 are 180 degrees out of phase.

Switching

To switch the amplifier IC on and off, a sample of the mixed audio signal is taken from mixer IC002 pin 8 and applied to the non-inverting input of the signal detector IC002 pin 4. The signal detect IC will amplify the 30mVp-p signal to 4Vp-p and apply it to the discharge switch which has an open loop gain. A clipping circuit (D005) cuts off the negative cycle of the sampled signal to prevent the discharge switch from being turned off.

When a signal of 25mVp-p or more is present at the input terminals of the super woofer, the inverting input of the discharge switch IC004 will be greater than 0.8Vdc (at the non-inverting terminal). The switch will act as a discharge path for C014 which had been charged up by Q004 (quick charge) when the unit had been plugged in. As long as there is a signal present the output at pin 1 will be 0V. When no signal is present, C014 will charge up to 7.8V through R28. The charging time is approximately 14 seconds due to the long time constant created by the 1MΩ resistor R28. The purpose of the delay is so that the woofer does not shut off during periods of time when there is no audio present in the television signal.

The output signal from the discharge switch is applied to the AUTO POWER-OFF IC004/pin 6. The auto peer-off circuit will invert the input signal and apply it to the mute switch Q003. The mute switch passes the power-off signal to the amplifier IC005/pin 1. When an audio signal is present, this pin will be HIGH, activating the amplifier.

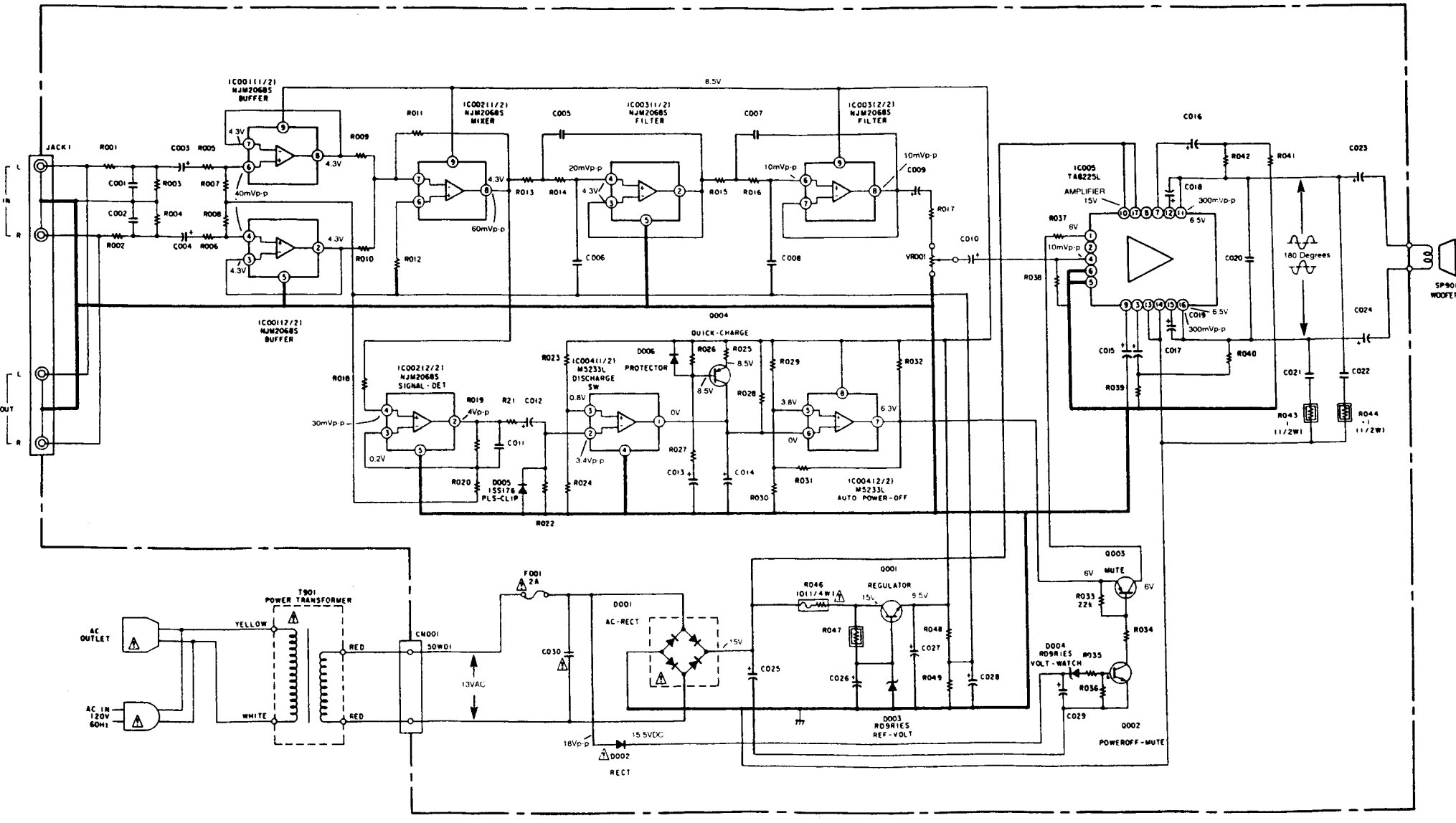
Mute Switch

The mute switch disables the amplifier when the AC voltage drops below 70Vac. In this case, the 9V zener diode D004 will become reverse biased and remove the base bias from Q002. Q002 will then turn OFF thereby turning mute switch Q003 OFF.

Troubleshooting Tips

The first step in troubleshooting any circuit are the must-haves. In this case they are:

1. Check for 15Vdc at the junction of R046 and C025.
2. Check for reg. 8.5Vdc at Q001/E (8.5Vdc regulator). Check for open R046.
3. Make sure that the collector of Q003 is HIGH when an audio signal is present.
4. Apply a 100Hz sinewave (0.775Vp-p) and signal trace.



SUPER WOOFER

BA-1 Audio Process

The left and right audio signals are output from the A/V switch, IC401, and are applied to the volume control IC404 pins 2 (left) and 14 (right). The volume control IC is controlled by the main micon, IC101, pin 59 (O-VOL). Both signals are amplified by the audio amp, IC251, and are applied to the speakers. To control the volume level, of the audio signal, a control signal of varying pulse width and amplitude is produced by IC101 as follows:

When the VOL+ button is pressed, IC101 pin 42 will go to 0.6Vdc (it is normally 5.2Vdc). IC101 will produce a 1.024kHz positive pulse at 3.3Vp-p from IC101 pin 59. As the volume increases, the pulse width and amplitude will increase until the signal is a negative going pulse at 8.8Vp-p. This signal charges up C063 and C461 through R093, R062 and R063. The result is a gradually rising dc voltage at IC404 pin 8 (volume 1).

Balance between the speakers, is maintained by a 1.024kHz square wave at IC101 pin 58. This signal charges up C064 through R080 to produce a 2.4Vdc level at IC404 pin 10 (volume 2).

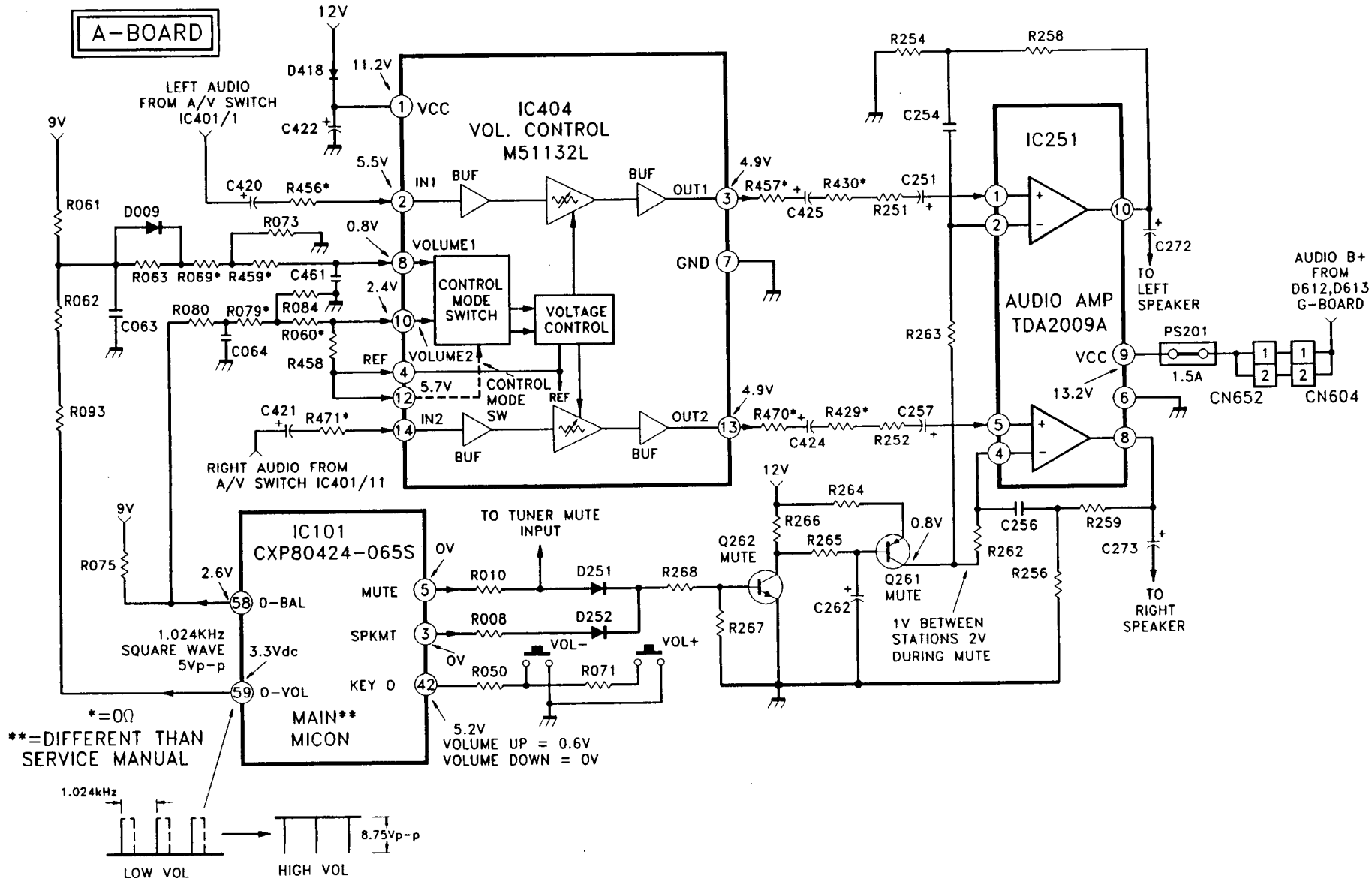
Muting

The audio signal is muted when scanning between stations and when the MUTE button on the remote commander is pressed. To mute the stations, IC101 pin 3 (SPKMT) will go HIGH. When the MUTE button on the remote commander is pressed, IC101 pin 5 (MUTE) will go HIGH. In either case, the following will occur:

- The base of Q262 (MUTE) will go HIGH, turning Q602 ON.
- Q262 will discharge C262 as long as Q262 is ON. This will turn Q261 ON which produces a positive voltage at its collector.

The voltage at the collector depends on which mute line is triggered. When muting between stations, Q262 is ON briefly. C262 will then discharge momentarily and Q261 will produce 1Vdc at its collector. When the MUTE button on the remote is pressed, C262 will discharge completely and Q261 will turn ON completely producing 2Vdc at its collector.

The voltage at the collector of Q261 will cause C254 to charge up through R254 and R263. This creates a "soft" mute since the muting voltage is gradually applied to the audio amp IC251 pins 2 and 4.



BA-1 AUDIO PROCESS

I^2C Data Format

In the last decade digital communication has taken a greater role in the control of the television chassis. To interface the digital system to the TV sub circuits, data, clock and chip select lines are connected in parallel from the main microprocessor to the many TV peripheral circuits. To direct data to a specific device, a specific chip select line is enabled which allows communication only with the selected device.

In the I^2C format however, each peripheral IC is connected to the main microprocessor via a two wire, data and clock, bus. Further each IC is assigned a unique address code. Data is then sent to a specific device by addressing the device with its uniquely assigned code, as appose to using a chip select. This permits only the addressed peripheral IC to accept data.

The data stream in the I^2C format contains the following items shown in the figure below:

- Start Bit.
- Address Word.
- Acknowledge Bit.
- At least one Data Word followed by an Acknowledge Bit.
- Stop Bit.

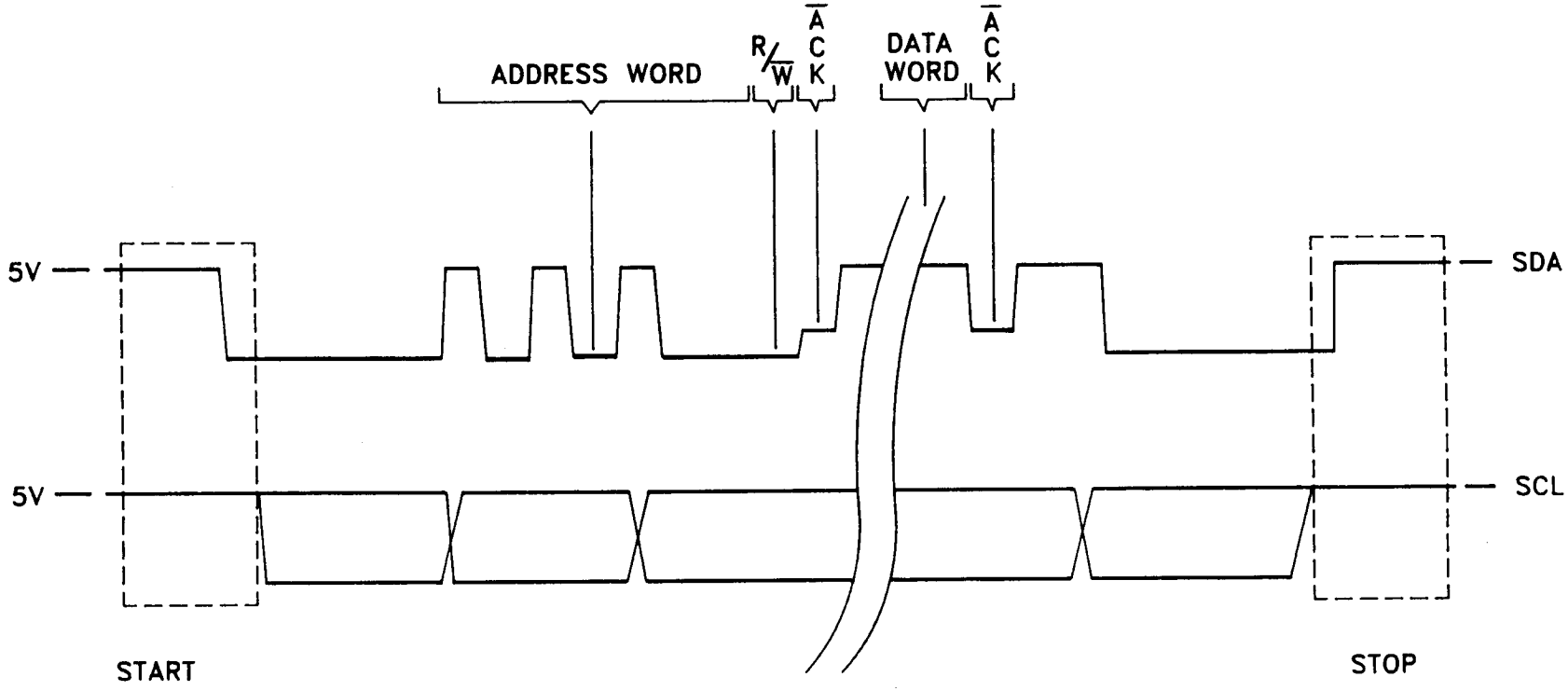
Note: The clock signal is always generated by the main micon.

Using this format eliminates the many separate chip select lines normally needed to address the peripheral devices — simplifying the hardware.

The format of the data on the I^2C bus is tightly controlled by the main micon. All devices connected to the bus other than the main micon are considered slaves and can only accept data when addressed. The slaves will recognize their address code when it is sent by the main micon. The slave must then acknowledge if communication with the main micon is to continue. As an example, when the main micon wants to send data to any device, it generates the bus clock and data stream signals to permit that transfer. Then the device being addressed must respond by acknowledging the main micon's request. The micon will then respond by sending the instructions it wants the slave to perform.

Within the format of the I^2C bus, unique situations occur at the start and stop of any data transfer. For instance, prior to the beginning of any data transfer the main micon will generate a start bit. As show in the figure below this is normally a HIGH to LOW transition of the data line while the bus clock is HIGH. Thus, all devices connected to the bus will recognize this as the beginning of the communication period. The bus is considered busy immediately after the generation of the start bit. Following the start bit the main micon will generate the address word. The address word is comprised of seven bits of data or highs and lows. The seven bit address word calls the device that the main micon wants to communicate with.

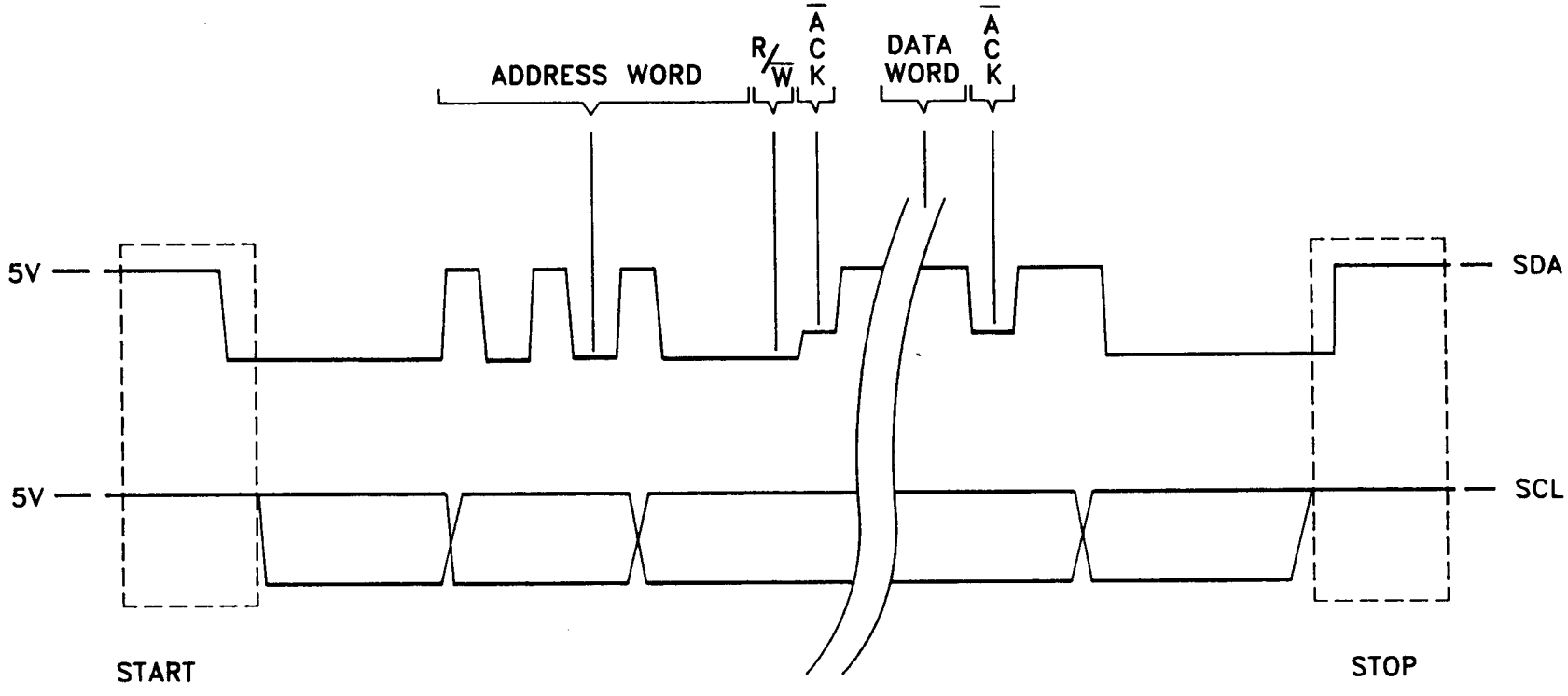
The address word is then followed by a read/write bit. If the main micon wants to write data, into the device being addressed, the read/write bit will be LOW. In the event that the main micon wants to read data from the device being addressed, the read/write bit will be HIGH. Following the address word the device being addressed will generate an acknowledge pulse. Data transfer followed by acknowledgement is mandatory in the I^2C format. During the acknowledgement period the main micon's data I/O port will assume a high impedance state. The data line will go HIGH because of external pull-up circuitry. The device being addressed must pull down the data line from its HIGH state to a LOW which signifies acknowledgement or receipt of the address information from the main micon. The main micon must detect the acknowledge pulse before it can send any additional data to the device. In the event the device does not acknowledge, the main micon will abort all further communications with the device.



I²C DATA FORMAT

Following the acknowledge pulse, data will be transferred in eight bit segments (eight bit data word). Afterwards, the device being addressed must once again generate an acknowledge pulse immediately following the receipt of each data word. Of course the data word may be an input or an output (read/write), to or from the main micon, depending on the read/write bit.

Any number of data words may follow a single address word. When data communication with the addressed device is finished, the main micon will output a stop condition or stop bit. The stop of data transfer is similar to the start condition. In this situation however, the data line will go from LOW to HIGH while the bus clock line is HIGH. The bus is considered to be free again (not busy) following the generation of the stop bit



I²C DATA FORMAT

I^2C Data Communication

As already mentioned, the AA-1 and BA-1 chassis utilize the I^2C format for data communication. This format uses a two wire (data and clock) bi-directional data bus structure. These two chassis share a common SONY microprocessor, IC101, for I^2C data transfer. Note: The AA-1 chassis service manual refers to this microprocessor as a Tuning Micon. The BA-1 chassis service manual refers to it as a PLL Control/Display IC. For the sake of simplicity, the two microprocessors will be referred to as a Main Micon in this course book.

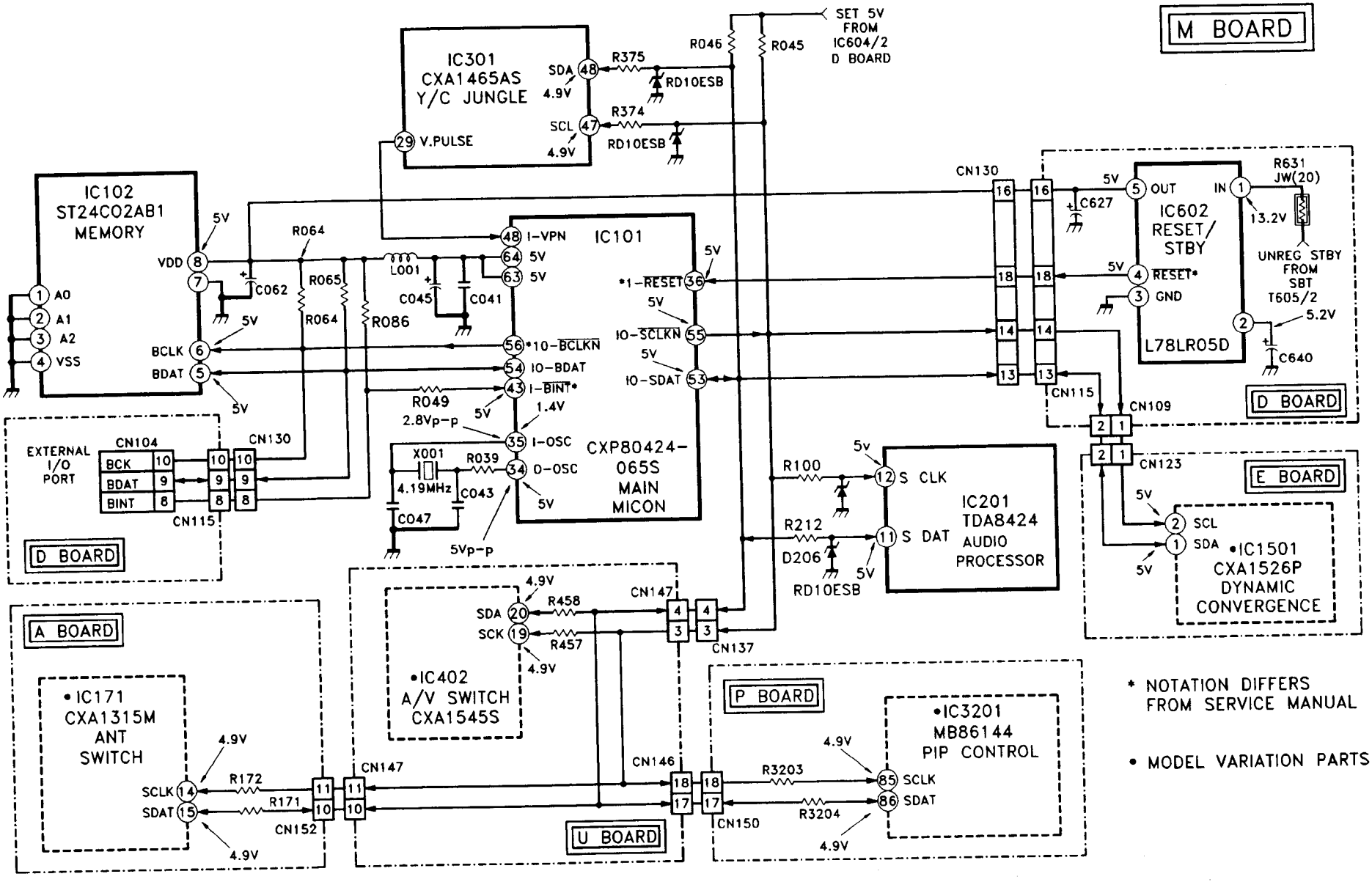
Data Exchange

Standby 5Vdc is applied from IC602 pin 5 to the main micon IC101 at pins 64 and 63 and to the memory IC102 at pin 8. Reset is applied from IC602 pin 4 to the main micon IC101 at pin 36. The I^2C data and clock ports, for the main micon IC101, are at pins 53 and 55 respectively. The data and clock signals are coupled from pins 53 and 55, to the peripheral ICs, for most of the set's functions. These include the following ICs:

- The Y/C jungle, IC301, on the M board.
- The audio processor, IC201, on the M board.
- The dynamic convergence, IC1501, on the E board.
- The PIP control, IC3201, on the P board.
- The A/V switch, IC402, on the UA board.
- The antenna switch, IC171, on the A board.

Once reset occurs, IC101 has main crystal activity present at pins 35 and 34. When the set is turned ON, IC101 outputs I^2C data and clock to the data bus. Unlike previous I^2C bus chassis, the non volatile memory, IC102 (EEPROM), is connected to the main micon, IC101, at separate ports which permits direct and isolated bi-directional data communication to take place for all read/write operations. This also eliminates the use of a data switch (used in previous chassis) to isolate the EEPROM and peripheral ICs before power ON. The EEPROM, IC102, functions are to store the set's alignment data, last channel watched, volume, color, and brightness settings for all input sources.

The external I/O port connector, CN104, is used to interface the I^2C bus to a design computer during the manufacturing process. The computer grabs control of the bus by setting the CN104 pin 8 (BINT) interrupt signal LOW (0Vdc) which allows the computer to send the set's alignment data to the non volatile memory IC.



IC² DATA COMMUNICATION

Troubleshooting

The very first step in troubleshooting microprocessor systems is to check all "must-have" conditions. These are:

Vcc 5Vdc at IC 101 pins 64 and 63.

Reset This is a 5Vdc delayed voltage input to IC 101 pin 36.

Clock This is a 4.19MHz 5Vp-p signal at IC 101 pin 34 and a 2.8Vp-p level at pin 35.

BINT This is pin 43 of IC101 which should be 5Vdc at all times. If LOW (0VDC), IC101 will only respond to inputs from an external device.

If a "must-have" is missing, troubleshoot and repair that problem before going any further. Since this data bus is shared by several devices throughout the system, it is not practical to try to interpret the data. Just make sure that there is data and clock activity present at a 5Vp-p level. If the data or clock signal is less than 5Vp-p, then look for a loading problem along the bus. Suspect a faulty diode or capacitor.

EEPROM Failures

EEPROM failures fall under the following three categories:

- The TV responds to power ON but has no raster or sound.
- The TV appears misaligned.
- Will not memorize a user define function setting or allow access to a user function.

The TV Responds to Power ON but has no Raster or Sound

When this is the symptom, the data or clock line may be loaded by the defective EEPROM causing the main micon to not communicate with the Y/C jungle IC. In this situation the TV will turn ON but will have a muted raster and no sound. However, high voltage will be present (evident by lit CRT filament). Additionally, other control functions such as channel change, volume up/down, input source select, etc., won't work.

The TV Appears Misaligned

When this is the observed symptom, it is quite probable that IC101 has loaded the set's alignment data, from its internal default data registers, to allow the TV to function. If this is the case, the default data will cause vertical centering, brightness, color hue, and color saturation levels to be wrong.

The TV may be re-aligned however, you will not be able to write the alignment data into the non-volatile memory (EEPROM) IC. Therefore, when ac is removed this data will be lost.

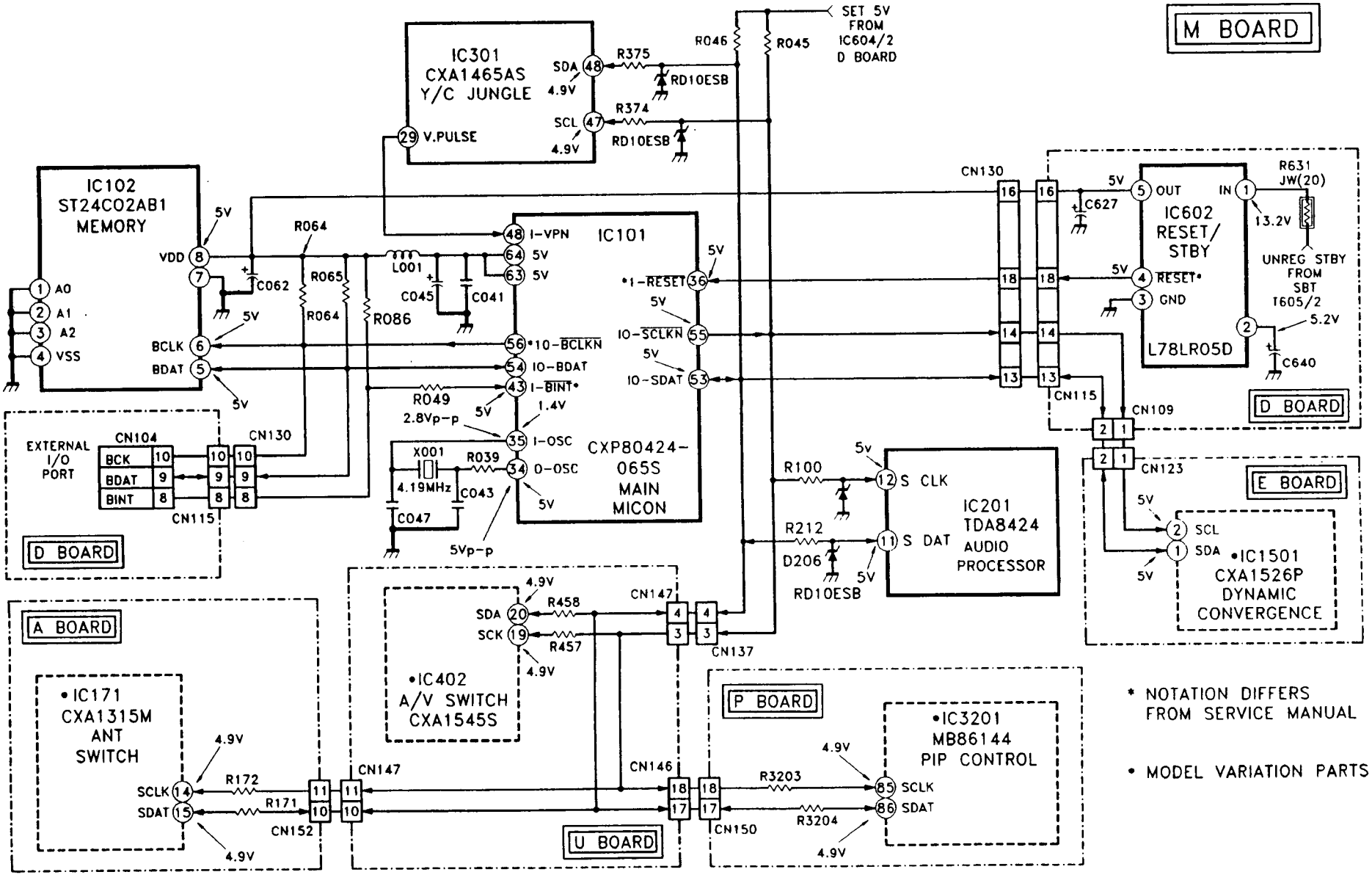
Will not Memorize a User Defined Function Setting or Allow Access to [illegible] Function

In this case the EEPROM will have partially failed so it will not allow some user functions to be recalled or memorized.

Replacing the EEPROM followed by a complete service alignment should restore normal operation. NOTE: Further troubleshooting information on this topic can be found at the end of this manual.

EEPROM Replacement Procedures

- Unplug the TV from the ac line.
- Replace the EEPROM.
- Reconnect the TV to the ac line.
- Enter the service mode by pressing the following keys on the remote controller: "DISPLAY" → "5" → "VOLUME +" → and "POWER". (You must press each key within a half second of each other).
- Enter the default adjustment data values, for each register, as listed in the service manual for the set. You can also enter the data values from another set of the same type.
- Fine tune the adjustments.
- ***Don't forget to write the adjustments to memory before exiting the service mode!***



IC² DATA COMMUNICATION

Vertical Deflection

The vertical deflection circuit provides the 60Hz sawtooth current, to the deflection coils, so that the beam will trace from the top to the bottom of the screen. The vertical deflection circuit is comprised of two stages. These are:

- The vertical oscillator (internal to the Y/C jungle IC301).
- The vertical output IC501 TDA8172 stage (The BA-1 chassis uses a SANYO LA7830).

The vertical deflection circuit also contains a sweep loss protection circuit Q314 and associated components. This circuit is used to prevent phosphor burns to the CRT by muting the video in the event the vertical deflection stage fails.

Operation

As shown in the diagram below, a composite sync signal is coupled from the emitter of Q302 (not shown), at a level of 1.4Vp-p, through C334 to IC301 pin 44 to the vertical sync separator section internal to the IC. The vertical sync signal is coupled to a vertical oscillator section where it is used to synchronize the internal vertical oscillator to 60Hz. The 60Hz sawtooth vertical drive signal is output, at a level of 1.3Vp-p, from IC301 pin 31 and is coupled through R508 to the vertical output IC501 pin 1. From pin 1 of the IC, the sawtooth signal is coupled to an internal differential amplifier. Normally the sawtooth voltage at the input of this IC is approximately 1.3Vp-p. The vertical sawtooth signal is amplified to approximately 52Vp-p and output from IC501 pin 5 to the vertical deflection coils.

To bring the pulses of the sawtooth signal up to the 52Vp-p level, C535 is charged by the flyback pulses generated from IC501 pin 3 through R537, D518 and D519 during the vertical scan period. This allows C535 to charge-up to the power supply voltage plus the flyback pulse 38 Vp-p level. During the vertical retrace period however, the charge stored in C535 is added to the power supply voltage at pin 6, thereby boosting the sawtooth signal to the 52Vp-p level. In other words, the power supply voltage is applied to the output stage during the vertical scan period, and the sum of the charge stored in C535 and the power supply voltage are applied to the output stage during the retrace period.

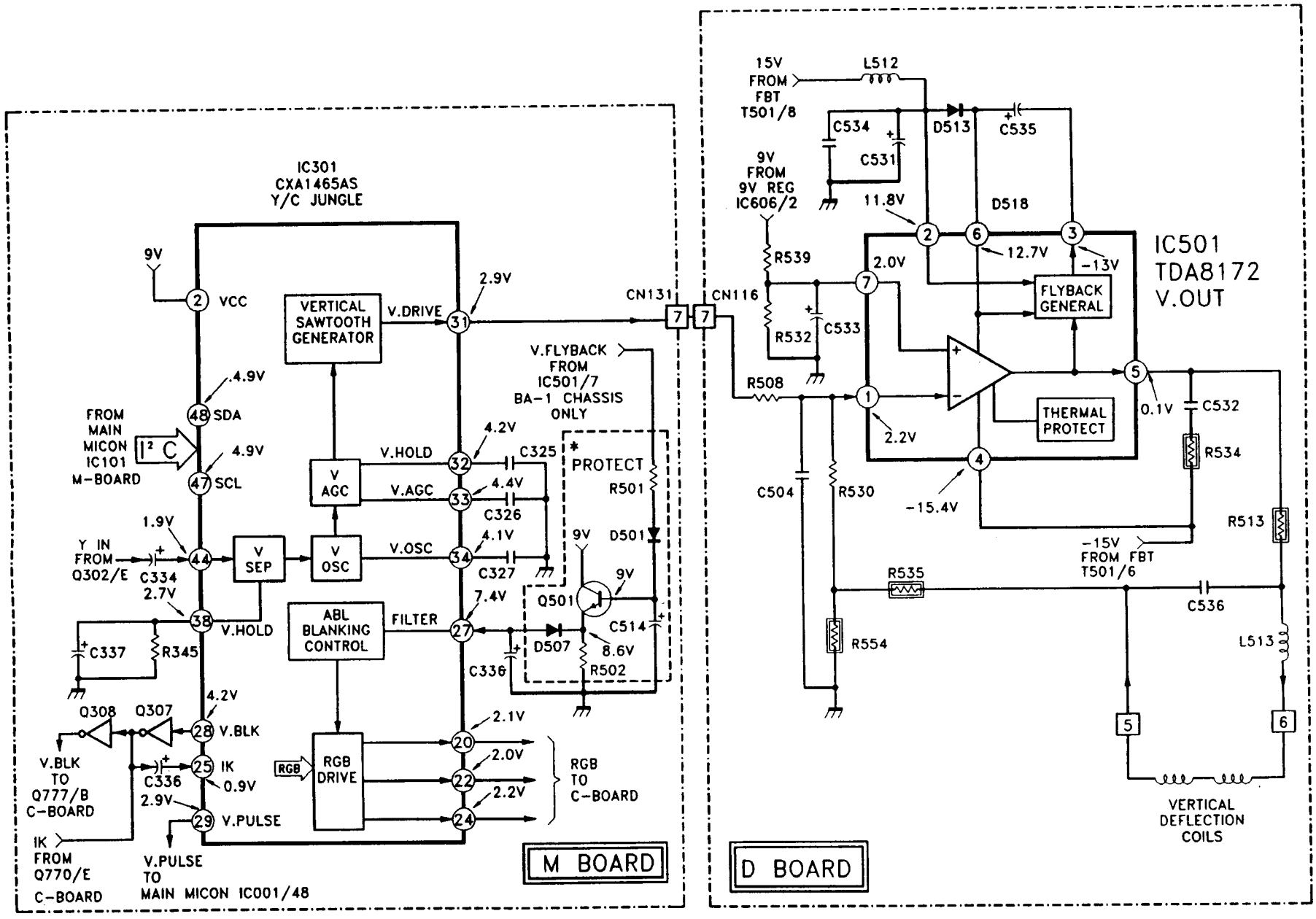
BA-1 Chassis Vertical Deflection

The BA-1 chassis uses a SANYO LA7830 IC for vertical deflection. Therefore it is not pin compatible with the IC used in the AA-1 chassis. The BA-1 chassis also has a vertical sweep loss sense circuit. A circuit description follows.

Vertical Sweep Loss BA-1 Chassis Only

The vertical sweep loss circuit is comprised of the following components: R501, D501 C514, Q501, D507 and C336. The purpose of this circuit is to sense the loss of vertical deflection. This is done by monitoring the retrace pulses generated by the internal flyback generator, at IC-501 pin 7. From IC501 pin 7 the vertical retrace pulses are coupled through R501, D501 and C514 to the base of buffer transistor Q501. D501 and C514 rectify the vertical retrace pulses to 9Vdc thereby turning Q501 ON. With Q501 ON, the emitter voltage will rise to 8.6Vdc. As a result, the blocking diode, D507, connected to the Y/C jungle at pin 27 is reversed biased and will remain OFF. With D507 OFF, IC301 pin 27 will remain at 7.4Vdc and the set will continue to function normally.

In the event vertical deflection is lost, the flyback pulses, from IC501 pin 7, will not be generated. In this situation the flyback pulses will not be detected and C514 will not charge to 9Vdc. Q501 will immediately turn OFF. With Q501 OFF, D507 is forward biased and will turn ON. As a result, IC301 pin 27 is pulled LOW (1.2Vdc) which triggers and internal muting circuit to remove RGB outputs from IC301 pins 20, 22 and 24.



*THIS CIRCUIT IS USED IN THE BA-1 CHASSIS ONLY

VERTICAL DEFLECTION

Troubleshooting

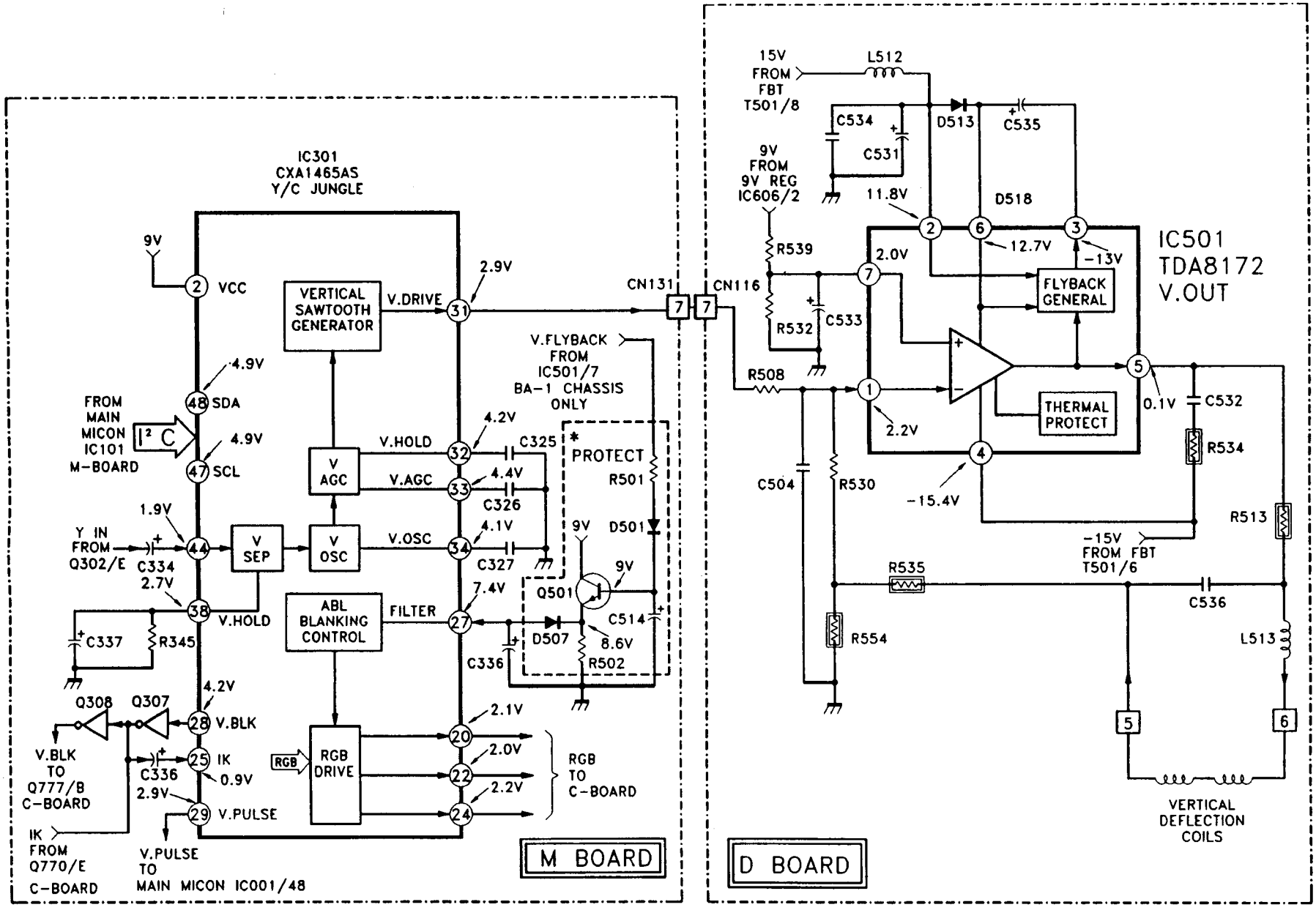
When servicing for loss of raster conditions, do the following checks:

Check for B+ (9Vdc) at IC301 pin 2 and for I^2C clock and data activity at IC301 pins 47 and 48. If data or clock activity is missing, isolate the possibly of signal loading on these pins before establishing that you have a defective IC. Check also for a 4.7Vp-p V. BLK signal from IC301 pin 28. If this signal is missing there can be no IK return signal input to IC301 pin 25 and the raster will be muted.

Check for 7.7Vdc at IC 301 pin 27. In the case of the BA-1 chassis If pin 27 is LOW (1.2Vdc) then unsolder D507 cathode end to temporarily defeat the sweep loss circuit. This will allow you to observe the symptoms on the screen as you proceed to troubleshoot the vertical deflection stage.

Check for +15Vdc at IC-501 pin 2 and -15Vdc at pin 4 and for 2Vdc at IC 500 pin 7.

Check for a 60Hz 1.5Vp-p sawtooth at IC301 pin 31 and IC501 pin 1 and for a 60Hz 38Vp-p retrace pulse at IC-501 pin 3 and a 60Hz 52Vp-p deflection signal at IC501 pin 5. If all appears okay, suspect the vertical deflection coils.



*THIS CIRCUIT IS USED IN THE BA-1 CHASSIS ONLY

VERTICAL DEFLECTION

Horizontal Deflection / FBT Scan Derived Voltages

The horizontal deflection circuit provides the 15,734kHz sawtooth current to the deflection coils so the electron beam will trace from left to right on the screen. It also generates the high-voltage required for picture tube operation. The horizontal deflection circuit is comprised of four sections. These are:

Horizontal Oscillator
Horizontal Drive
Horizontal Output
High-Voltage Circuit

The horizontal deflection circuit is also comprised of sub-circuits that include the following:

ABL
X-Ray Protect
Pincushion Correction

Operation

As illustrated in the diagram below, the horizontal sawtooth signal is generated from the Y/C jungle IC301 pin 37 (not shown) on the M board. This signal is coupled through horizontal pre-driver, Q502, and horizontal drive transformer, T502, to drive the horizontal output transistor Q591. The horizontal output transistor is connected to the flyback transformer, T501, and to the horizontal deflection coils. The horizontal deflection coils return is connected to the horizontal centering and the pincushion modulation circuits. These circuits are discussed later on.

The horizontal flyback pulse (H pulse) is coupled through the ac divider network C518, C517, C515, voltage limiters R514 and D512 to the main micon IC101 pin 47 (not shown) on the M board. The main micon uses this pulse to generate and to synchronize the on screen display characters information displayed on the screen. The horizontal flyback pulse is also coupled to the internal Y/C jungle IC301 pin 39 (not shown) horizontal phase detector on the M board. There the horizontal flyback pulse is compared to the video signal's horizontal sync pulses coupled to the Y/C jungle IC301 pin 45 (not shown) for automatic frequency control (AFC). In turn, the output of the phase detector circuit maintains an internal horizontal voltage control oscillator (VCO) locked to the NTSC 15,734kHz color frequency.

The horizontal pulse is also sent to the pincushion modulation circuits to correct the east/west horizontal deflection picture distortions.

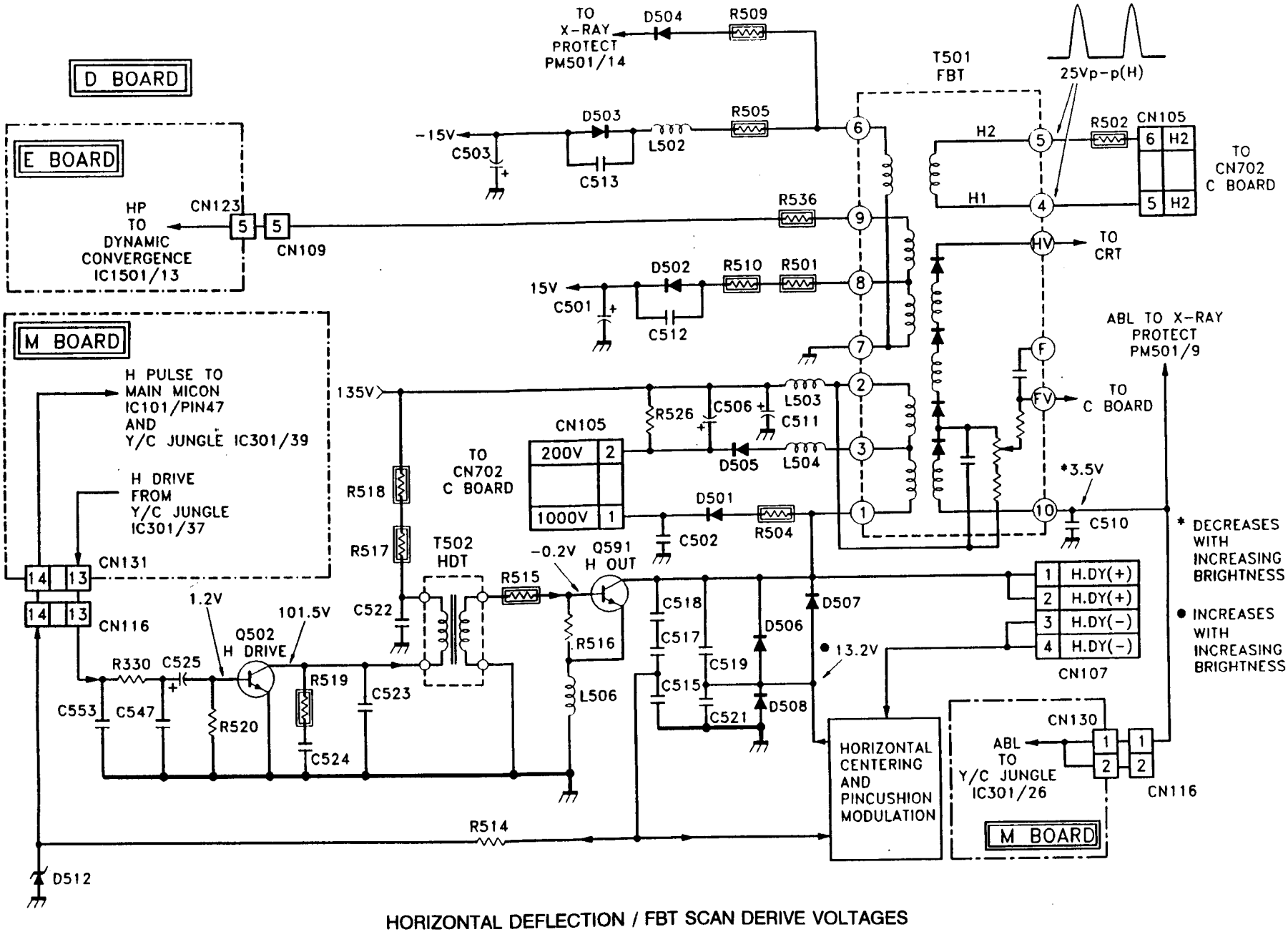
Flyback Scan Derived Voltages

The flyback transformer, T501, generates the many scan derived supply voltages for the following circuits:

- 200Vdc, from pin 3, which provides the bias voltage to the CRT RGB drives on the C board.
- 1000Vdc, from pin 1, which provides the G2 bias to the CRT C board.
- 15Vdc, from pin 8, which provides the bias to the vertical deflection IC and the pincushion modulation drive circuits.
- -15Vdc, from pin 6, which provides the bias to the vertical deflection IC.
- 126Vdc, also from pin 6, which provides the x-ray detect sample voltage to the PM501 module.
- 6.2Vac heater voltage, from pins 4 and 5, to the CRT C board.

The flyback transformer also generates the following:

- High voltage, from the HV pin to the CRT anode.
- Focus voltage, from the FV pin, to the CRT C board.
- ABL, from pin 10, to the pincushion modulation circuits, the PM501 module for detecting excess picture tube current, and to the Y/C jungle IC on the M board.
- HP signal, from pin 9, to the dynamic focus circuits on the E board.

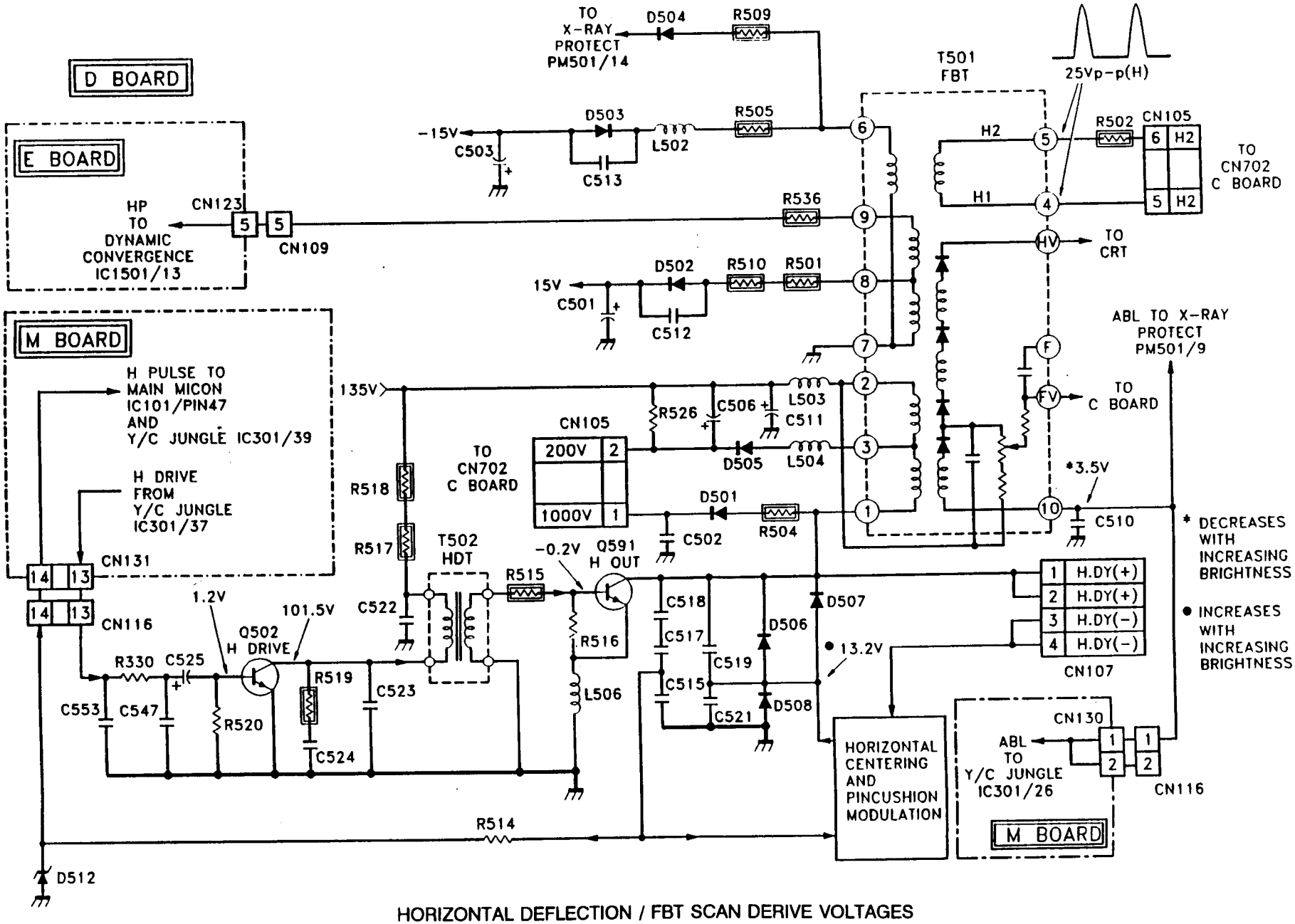


HORIZONTAL DEFLECTION / FBT SCAN DERIVE VOLTAGES

Troubleshooting

When servicing hi-voltage problems or no raster conditions, you should confirm proper operation of the horizontal circuitry. You can do this quickly by looking for a lit CRT filament. If the filament is missing, it is a good indication that the horizontal section has failed. You can confirm the operation of this circuit by performing the following checks:

- Check for 135Vdc at T501 pin 2. If it is missing then check the power supply for faulty components.
- Check horizontal output, Q591, horizontal driver, Q502, and damper diodes D506, D508 and D507 for possible PN junction failure. A simple front to back ratio test performed with a multimeter can quickly show the condition of the transistors and diodes. If the horizontal transistor reveals a short, replacing it at this point requires that you check the pincushion output transistor (not shown) and that you suspect the flyback transformer, T501, for possible failure.
- Check IC301 pin 37 for a 4Vp-p horizontal drive signal. It should resemble a square wave.



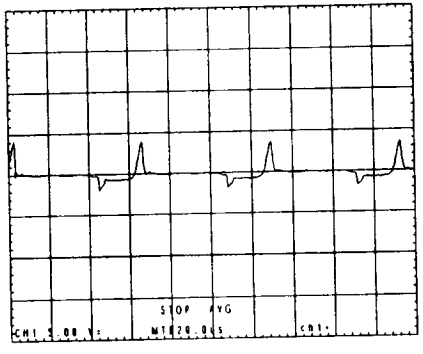
HORIZONTAL DEFLECTION / FBT SCAN DERIVE VOLTAGES

BA-1 Chassis Horizontal Troubleshooting

If the power supply shuts down due to a defect in the horizontal/flyback section, it will be necessary to isolate the flyback transformer from the rest of the circuits which are fed by the 115Vdc supply. To do this, lift one end of L503 (C2 section in the board layout) and connect a dc power supply to T504 pin 4. Connect your X10 scope probe to the collector of H.OUT drive Q551. Set your scope as follows.

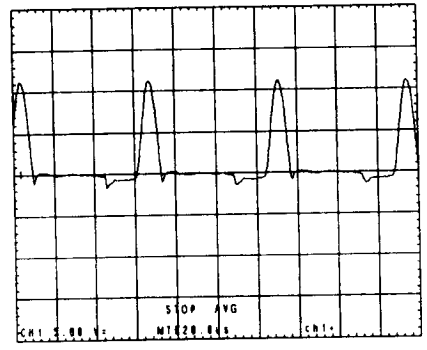
VERT: 5v/div
HOR: 20usec/div

Turn the set on and observe your scope. You should observe a 7.3Vp-p waveform as shown below, with no voltage applied to the horizontal flyback transformer T504 pin 4.



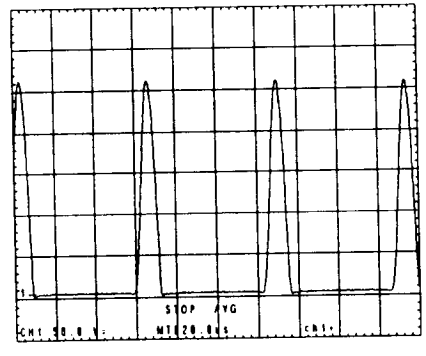
Q551/C 7.3Vp-p
5V/div. 20usec/div

Next, increase the external power supply voltage to 1Vdc and observe the waveform. You should have a 13.8Vp-p pulse at 15.75kHz as shown below.



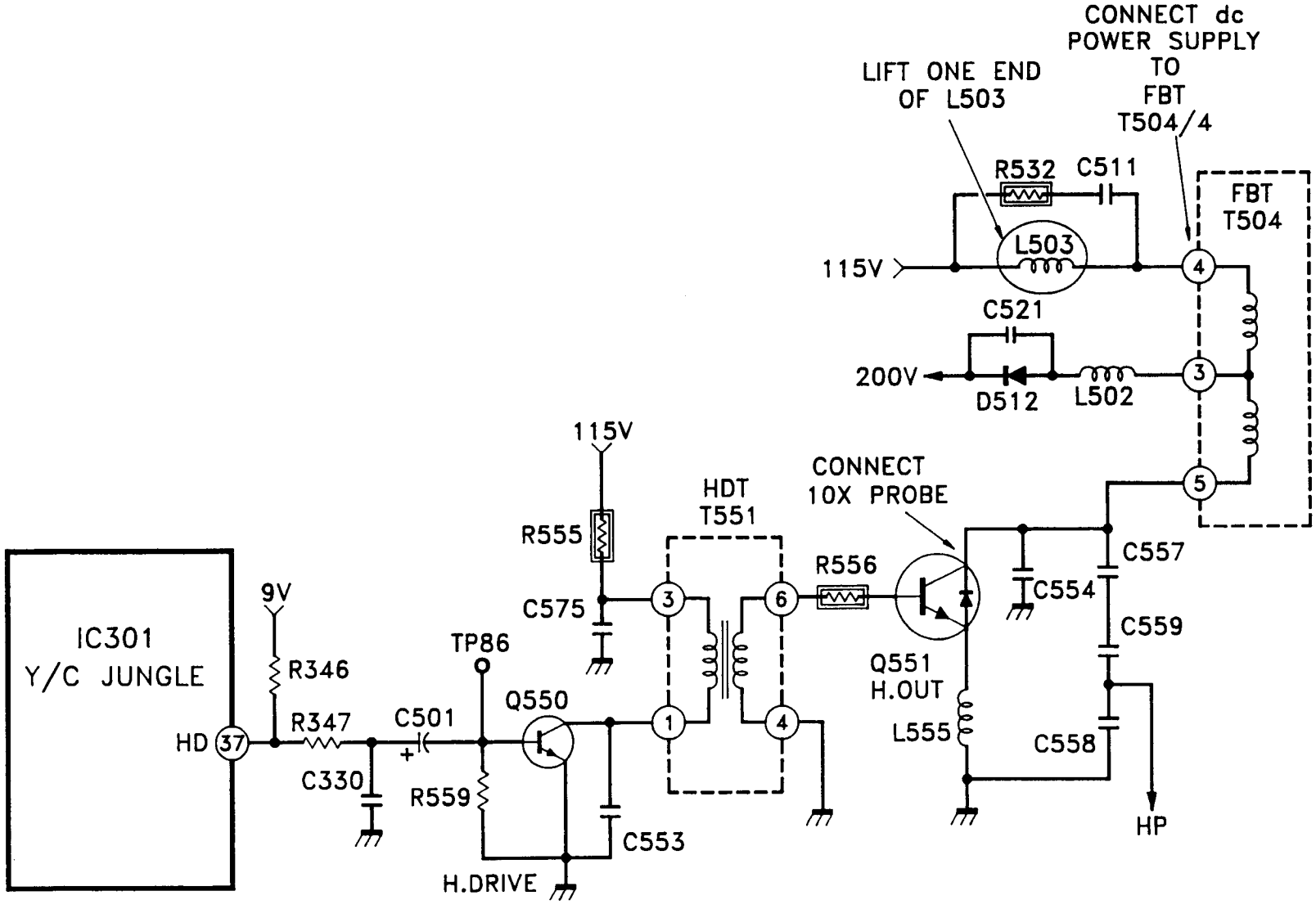
Q551/C 13.8Vp-p
5V/div 20usec/div

Slowly increase the external power supply voltage to 30Vdc while observing the waveform. The waveform pulse should increase, in amplitude, to 268Vp-p without any waveshape distortion as shown below.



Q551/C 268Vp-p
50V/div 20usec/div

Continue to increase the external power supply voltage until shut down occurs. You can now begin isolating each section of the flyback and horizontal drive stage until the defective component is found.



BA-1 CHASSIS HORIZONTAL TROUBLESHOOTING

Pincushion Modulation

The pincushion correction circuit, often referred to as the east/west correction circuit, is used to correct for the physical left to right screen distortion or bowed-in effect in the picture. To correct for the distortion problems, this circuit utilizes a pincushion modulation circuit to increase the horizontal deflection current at the center of the raster. This has the effect of dynamically increasing the electromagnetic field through the yoke to automatically stretch the horizontal width of the picture at the regions where the raster is compressed inward.

Operation

Pincushion amplifier, IC504, and transistors Q505 and Q503 form the pincushion correction circuit. The circuit works as follows: The parabolic correction signal (E/W signal) is generated from the Y/C jungle IC301 pin 30 on the M board. From pin 30 the parabolic signal is coupled through connectors CN131 and CN116 pins 8 and through R543 to the pincushion differential amplifier, IC504, at pin 6. The parabolic signal is amplified within IC504 and is output from pin 7. From pin 7 the parabolic correction signal is coupled to the base of pin driver, Q505, where it is inverted and amplified, and output from its collector. From the collector the parabolic correction signal is coupled through R566 to the base of the pin output transistor Q503.

The pin output transistor, Q503, collector is connected through L510 to the junction of damper diodes D506 and D507 and through C530 to the pincushion modulation transformer, T503. This allows the pincushion circuit to modulate the deflection output and independently vary the horizontal yoke drive current. The parabolic correction signal is timed with the E/W signal input to IC504 pin 6 and the H pulse signal coupled from the collector of the horizontal output transistor Q591 to IC506 pin 5 . This allows the deflection current to be maximized when scanning at the center of the screen and progressively reduced when the top and bottom of the screen is scanned.

D510, R522, R506, S502, D511, R523, S501, R512 and the 135Vdc line form the horizontal centering circuit. D510 and D511 rectify the ac yoke current to allow a small dc current to flow through the deflection coils. D510 subtracts from the 135Vdc supply line voltage to shift the picture to the right on the screen. D511 adds to the 135Vdc supply line voltage to shift the picture to the left on the screen. S501 and S502 can be configured to move the picture to either the left or to the right on the screen. S501 and S502 have no effect on the picture in the neutral (center) setting.

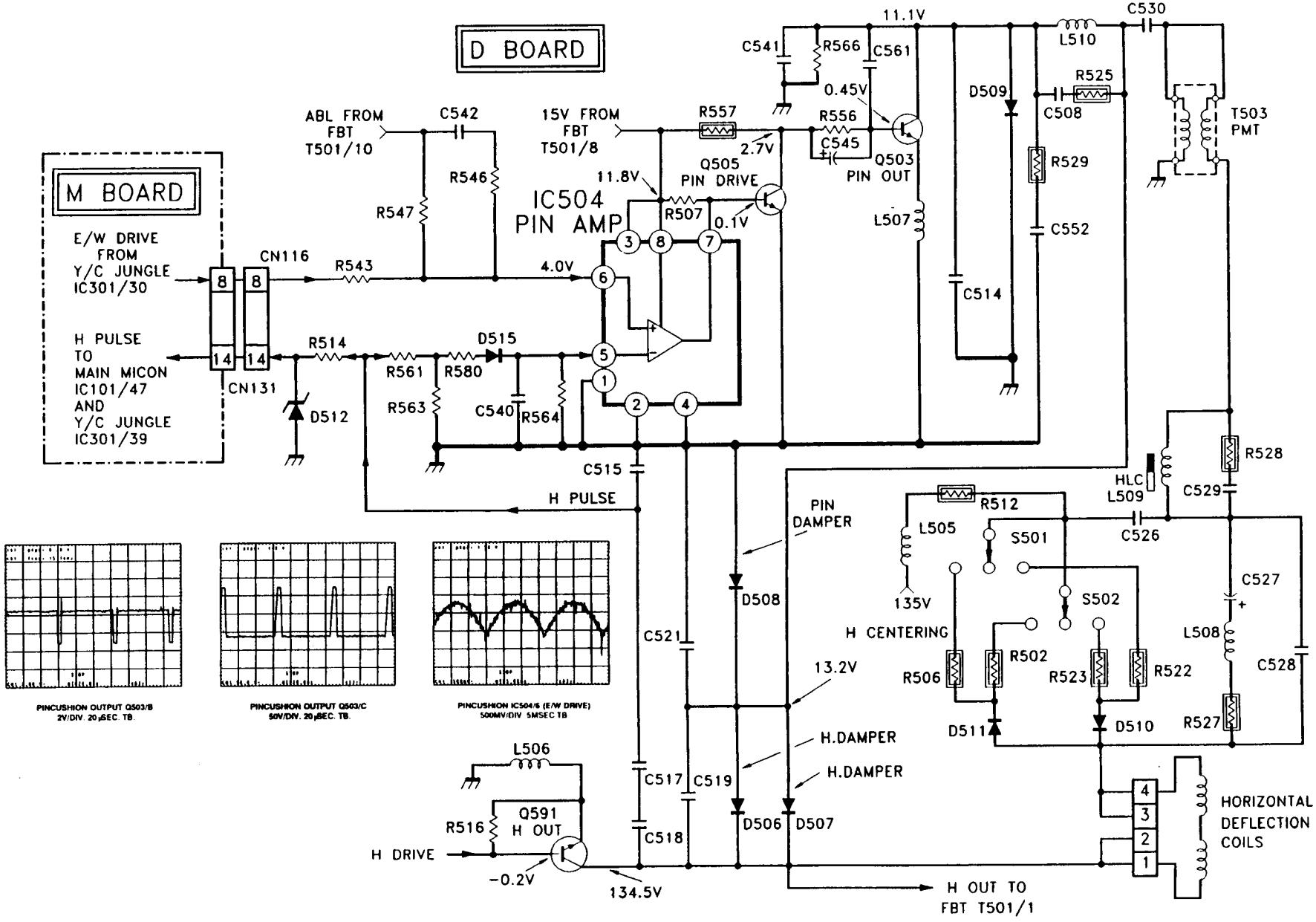
BA-1 Chassis Pincushion Modulation

The pincushion circuitry used in the BA-1 chassis is simpler. This chassis uses a single pin output transistor and does not require a pincushion modulation transformer due to the much smaller circuit current requirements. The circuit is very similar to the one found in the ANU-2 chassis. A complete circuit description can be found in the CTV-18 course book.

Pincushion Troubleshooting

Pincushion circuits do not fail often because the pincushion circuit handles small amounts of current. If the pincushion circuit fails, it will cause a physical distortion or bowed in effect in the picture. A shorted pincushion output transistor causes excessive current to flow in the flyback and horizontal output circuits which increases the chances for breakdown in these components. To locate a problem in this section do the following checks:

- The pincushion amplifier, Q503, and pincushion driver, Q505, for PN junction failure.
- L510 for signs of overheating, which will cause a change in the impedance of the coil and cause Q503 to overheat and fail.
- Y/C jungle IC301 pin 30 (e/w drive) for a 2.5Vp-p parabolic signal.



PINCUSHION MODULATION

X-Ray / Over Current Protect

The x-ray and over current protect circuit serves to safeguard the set from excess x-radiation emissions, from abnormal high voltage operation, and from power supply current overloads. To do so, the x-ray circuits monitors the 126Vdc flyback scan derived supply voltage, the picture tube anode current (ABL), and the 135Vdc power supply line current (over current). If for any reason these circuits exceed a predetermined level, the x-ray and over current circuit operates to shut OFF the set.

Operation

PM501 is the shutdown protect circuit. B+ to the PM501 protect module is applied, from the rectified 135Vdc line, to pin-5 to bias this stage. To sense high voltage, a sample of the scan derived +126Vdc line, from the flyback T501 pin 6, is applied to PM501 pin 14. The voltage from T501 pin 10 is coupled to internal differential amplifiers, which set the high voltage threshold level to trigger shutdown. In the event that the 126Vdc scan derive voltage exceeds 129Vdc PM501 pin 1 will go LOW (0Vdc). With pin 1 LOW the following occurs:

- The relay drive, output from the main micon IC101 pin 4, is shunted to ground through R632, R645 and the internal PM501 pin 1 latch circuits.
- The voltage at R645, R632 and D628 junctions goes to 0.7Vdc.
- Relay drive, Q604, base voltage goes to 0Vdc causing Q604 to turn OFF de-energizing the relay.

With the set in shutdown the standby supply 5Vdc continues to supply power to the main micon IC. In turn the main microprocessor IC continues to output a relay drive signal sourcing the internal PM501 latch circuits. The relay power OFF condition is held until the set is turned OFF or ac power is removed.

The picture tube anode current (ABL), output from the flyback transformer T501 pin 10, is sensed as a voltage at PM501 pin 9. Normally as anode current through the flyback increases (high picture brightness), the voltage

is between 1.5Vdc (white screen) and 8.5Vdc (black screen). From T501 pin 10 this voltage is coupled to internal differential amplifiers which set the ABL threshold level to trigger shutdown. In the event the ABL voltage goes too LOW (-14Vdc) PM501 pin 1 will go LOW (0Vdc) and operates to shut OFF the set as described earlier.

The 135Vdc line current is sensed across resistor R654. R654 is connected through R655 and R650 to PM501 pins 5 and 7. A current overload, in the 135Vdc supply line, will cause a large current to flow through R654. This will generate a voltage drop across PM501 pins 5 and 7. The voltage drop is coupled to internal differential amplifiers which set the over current threshold level to trigger shutdown. As a result, PM501 pin 1 will go LOW (0Vdc), and operates to shut OFF the set as described before.

Troubleshooting

There are three causes for power supply shutdown. These are:

- High voltage.
- ABL.
- Over current.

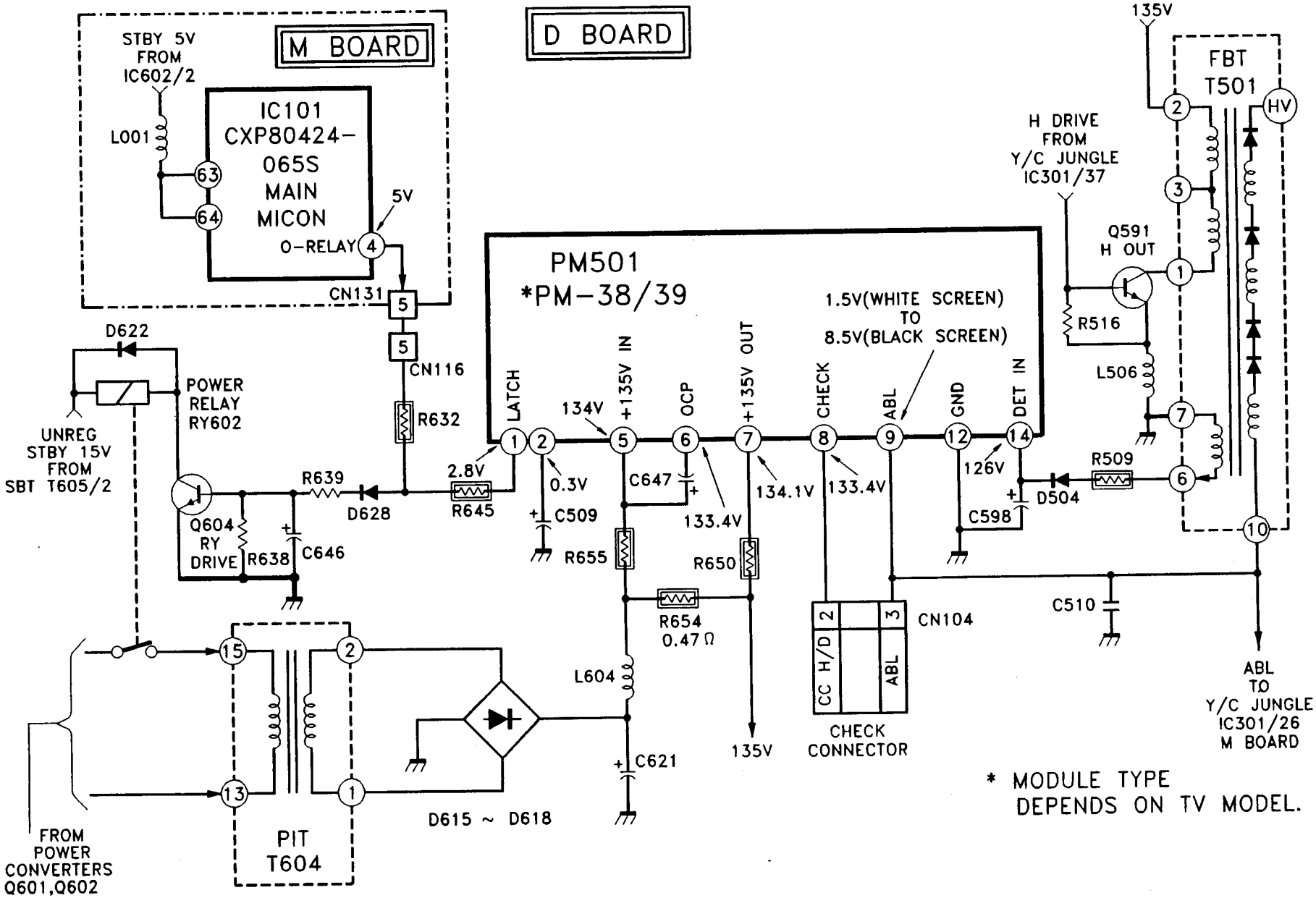
You must isolate these three causes to determine the faulty section. To do so do the following checks:

High Voltage

Measure the voltage input to PM501 pin 14. If it exceeds 129Vdc, check the power supply 135Vdc line. If this voltage exceeds 135Vdc, refer to the regulation/shutdown troubleshooting section in this manual. If okay, suspect the flyback,T501, and the horizontal drive signal to Q591.

ABL

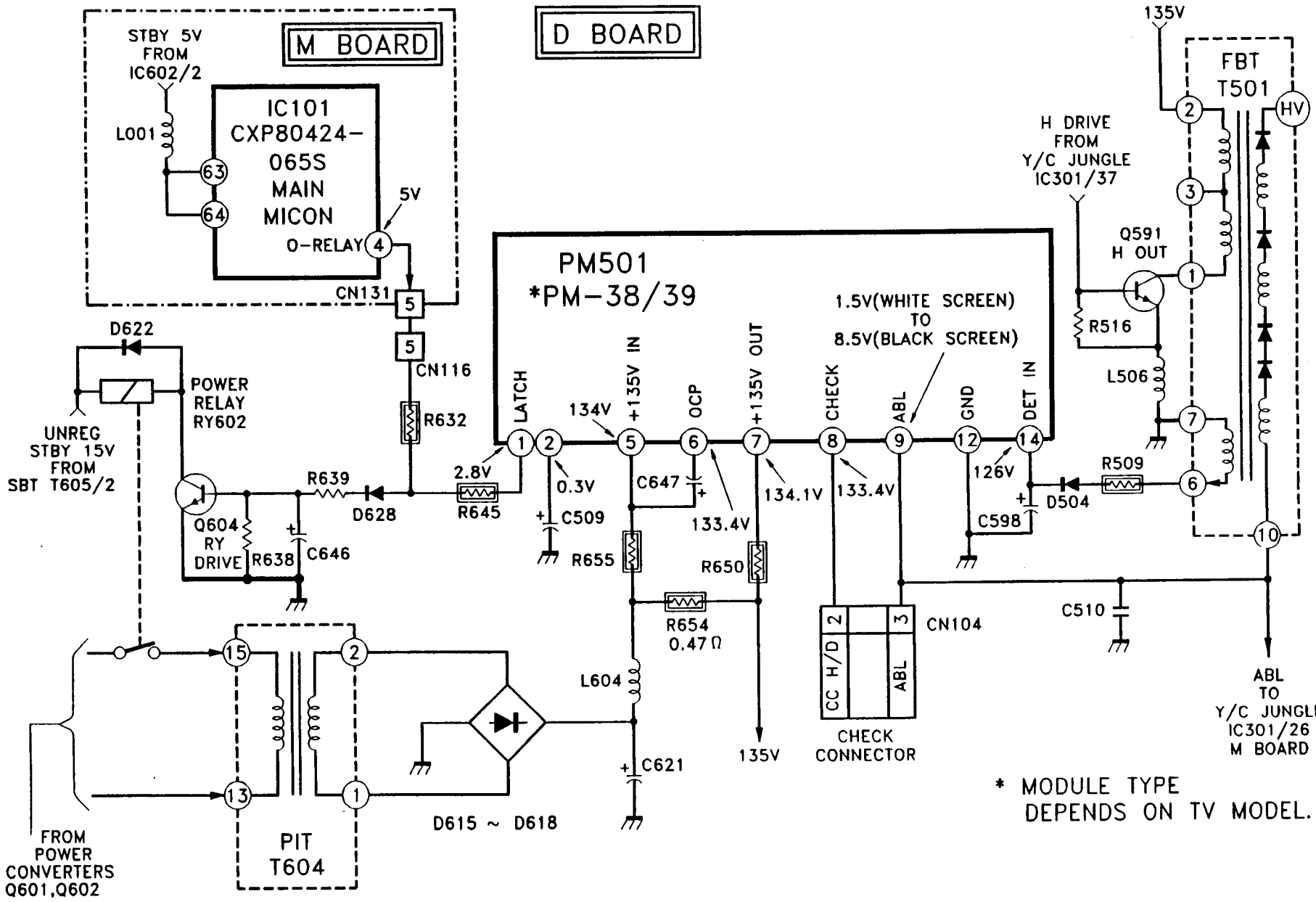
Measure the voltage input to PM501 pin 9. This voltage should not read negative at any given time. If it does, suspect a faulty picture tube. You can isolate the picture tube, by disconnecting the C board. If ABL measures 1.2Vdc, there will be a white only raster display.



X-RAY / OVER CURRENT PROTECT

Over Current

Measure the voltage across R654. If it measures more than 1.2Vdc suspect a shorted horizontal output transistor,Q591.



X-RAY / OVER CURRENT PROTECT

Automatic Cathode Bias Block

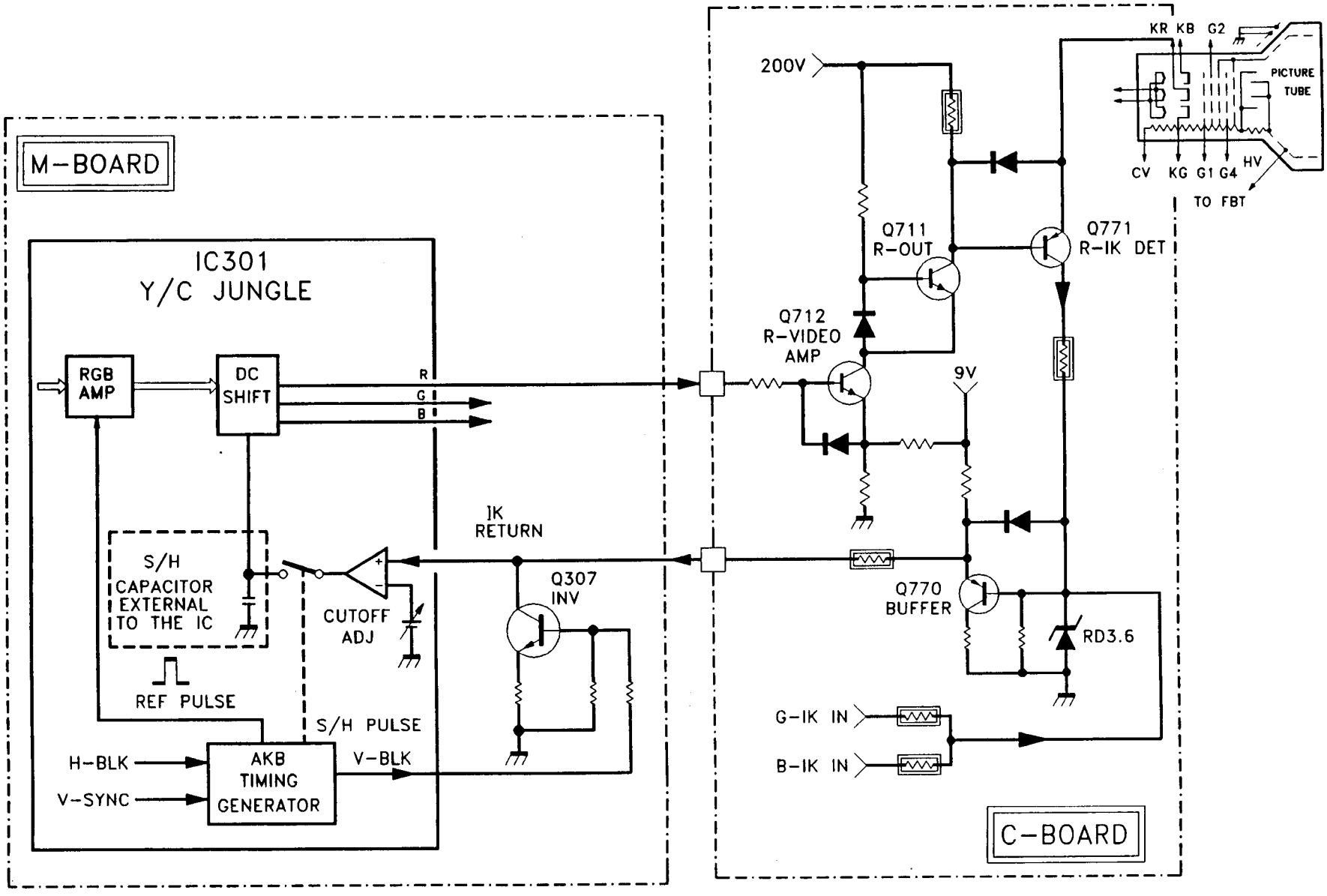
The AA-1 and BA-1 chassis utilize an Automatic Cathode Bias (AKB) system to compensate for CRT tolerances and to improve color temperature drift problems which occur during the life of the picture tube. To do this dynamic circuits are employed to monitor the cathode current (IK) of each color gun and correct the dc bias to each drive to maintain proper grey scale.

The AKB system monitors three reference pulses during a period called the AKB processing period. This processing period occurs for three horizontal lines, in both fields, just prior to active scan. During this period, the AKB circuit generates a reference pulse from the Y/C jungle RGB output pins to the CRT drives. The reference pulses require vertical and horizontal signals so they can be properly timed into the inactive portion of the composite video signal.

When the AKB pulse is generated, it causes the CRT to conduct for a short instance. It is during this brief CRT conduction time that a cathode current (IK) measurement period occurs. This IK current generates a dc voltage as it is passed across the biasing resistor connected at the base of the IK buffer stage. The resulting dc voltage is buffered and input to the Y/C jungle IC.

The IK buffer also passes the green and blue IK currents, to the Y/C jungle, in sequence with the red IK current. Within the Y/C jungle the individual RGB IK voltages are compared to an internal dc reference voltage. The result of this comparison generates a voltage charging an external sample and hold capacitor. The voltage held in the capacitor is coupled to an internal dc shift circuit. The dc shift generates an RGB offset bias voltage, to the respective color drive. From this loop the Y/C jungle IC compares the CRT cathode currents (IK) to the AKB internal cutoff reference bias, and generates a dc shift from the Y/C jungle RGB output lines. Note: By design, if any sample and held voltage is less than 4.2Vdc, the picture tube is automatically blanked (black raster).

Transistor Q307 controls the IK input period, to the Y/C jungle IC, by application of the vertical blanking pulse output from the internal AKB timing generator. This ensures that the IK measurement process occurs only during the vertical blanking interval and not throughout the picture's active scan interval. If this was not done, the IK circuitry would continuously perform gray scale adjustments, which would then result in the coloring of the video scene.



AUTOMATIC CATHODE BIAS BLOCK

Automatic Cathode Bias

The automatic cathode bias (AKB) circuit is shown in the diagram below. Note: The red AKB section is considered the main or reference circuit. Therefore, the red AKB circuit is used in describing the operation for the blue and green AKB bias section as well.

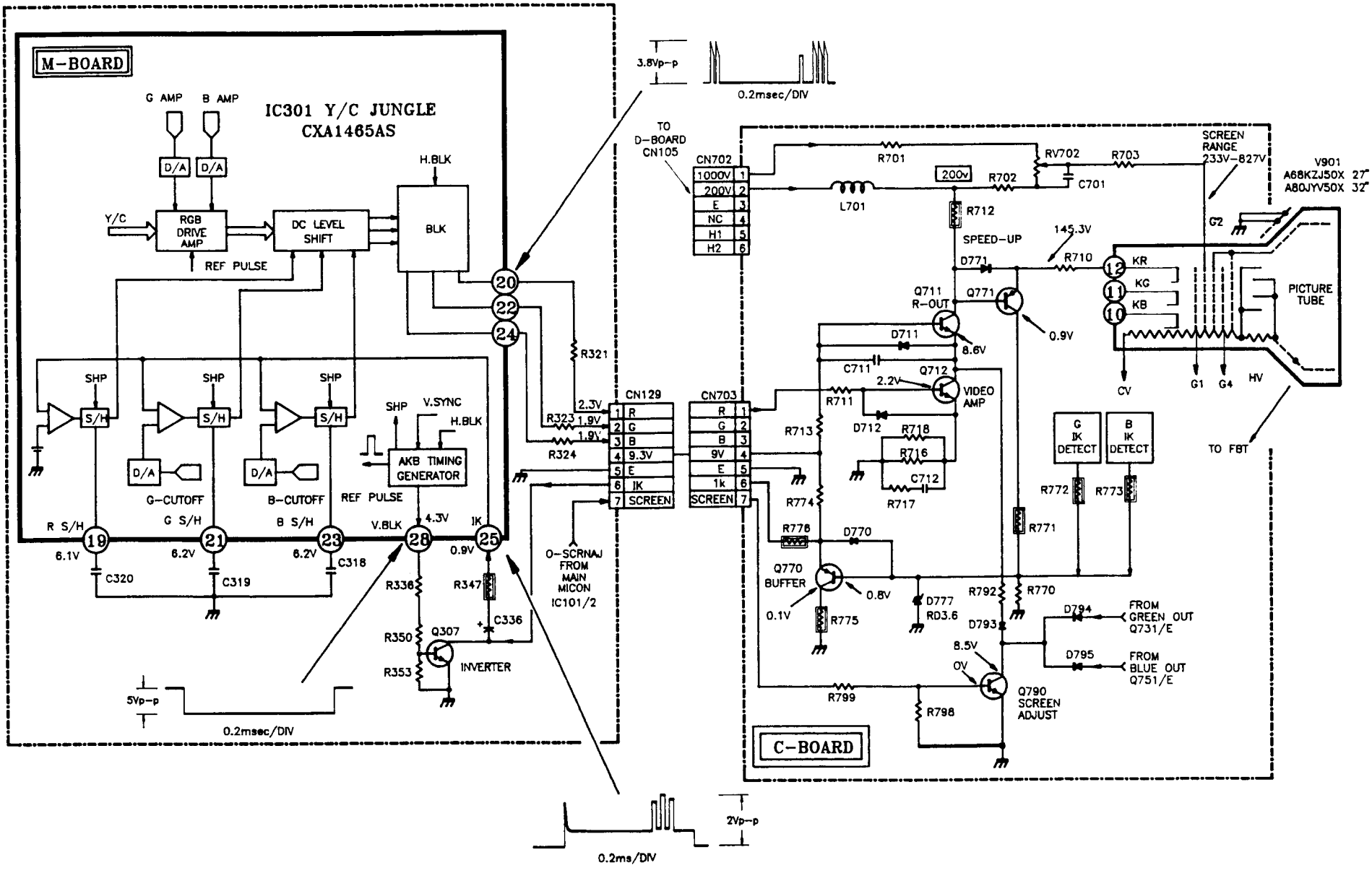
Referring to the diagram the AKB pulses, generated by the AKB timing generator inside IC301, are output at IC301 pins 20 (R), 22 (G), and 24 (B). As already mentioned earlier, the AKB timing generator synchronizes these pulses utilizing the horizontal and vertical pulses generated inside the Y/C jungle IC. The timing of these pulses is critical and the loss of any of these results in a blanked raster (black raster). These three pulses are generated sequentially within the vertical blanking period for a duration of three horizontal lines just prior to the active scan period. The position of the IK reference pulses within the vertical retrace period can be changed by altering adjustment address REF during the set's initial alignment process. However, this position is a factory setting which normally does not require any further readjustment. Altering the data at this address will produce three distinct retrace color lines per field to appear faintly at the top of the screen.

The red AKB pulse is coupled from the Y/C jungle pin 20 through video amp Q712, red output drive Q711, and the red IK detect Q771 to the cathode of the red picture tube gun pin 12. This pulse sets up a reference point for measuring the CRT cathode current. Application of this pulse allows the picture tube to conduct heavily resulting in increased cathode current.

When the picture tube conducts, the CRT current flows through IK detect Q771, R771 and R770 generating an IK voltage across R770. This voltage is then coupled through Q770 buffer base to emitter, R776 and to the Y/C jungle IC301 pin 25. From pin 25 this voltage is coupled to an internal comparator. The comparator is used to compare the IK voltage to a fixed internal red cutoff reference voltage. The resulting output voltage is used to charge the external sample and hold capacitor, C320, at IC301 pin 19. The voltage held in the capacitor is coupled to a dc shift circuit. As a result the dc shift will add an offset dc bias, to the red video signal, which dynamically adjusts the red drive to the picture tube.

The IK voltage for the green and blue color guns are also coupled to their respective AKB detect circuits within the Y/C jungle IC. The resulting detected voltages are also compared to internal green and blue cutoff voltage references and coupled to their respective sample and hold capacitors at pins 21 and 23. Proper bias to the green and blue color guns is maintained by charging and discharging their respective capacitors. The resulting dc shift is used to dynamically offset the bias to the respective color picture tube gun. Thereby controlling the color temperature of the picture tube.

Inverter Q307, connected to IC301 pin 25, turns ON during the active scan interval thereby grounding the return voltage from the IK detectors. IC301 pin 28 couples a vertical blanking pulse to the base of the inverter, Q307, to time the Q307 ON period. This circuit ensures the IK corrections take place only during the vertical retrace period and not during active scan which would tint the color picture. The CRT's G2 grid adjustment, RV702, is connected to the 1000Vdc through R701 and to the 200Vdc scan derived voltage through L701 and R702. The 1000Vdc and 200Vdc supplies are output from the flyback T501 pins 1 and 3 (not shown) respectively on the D board. The setting of this control determines the relative brightness balance between the shades of grays of the raster. The +200Vdc scan derived voltage line also provides regulated B+ to the CRT's RGB drives.

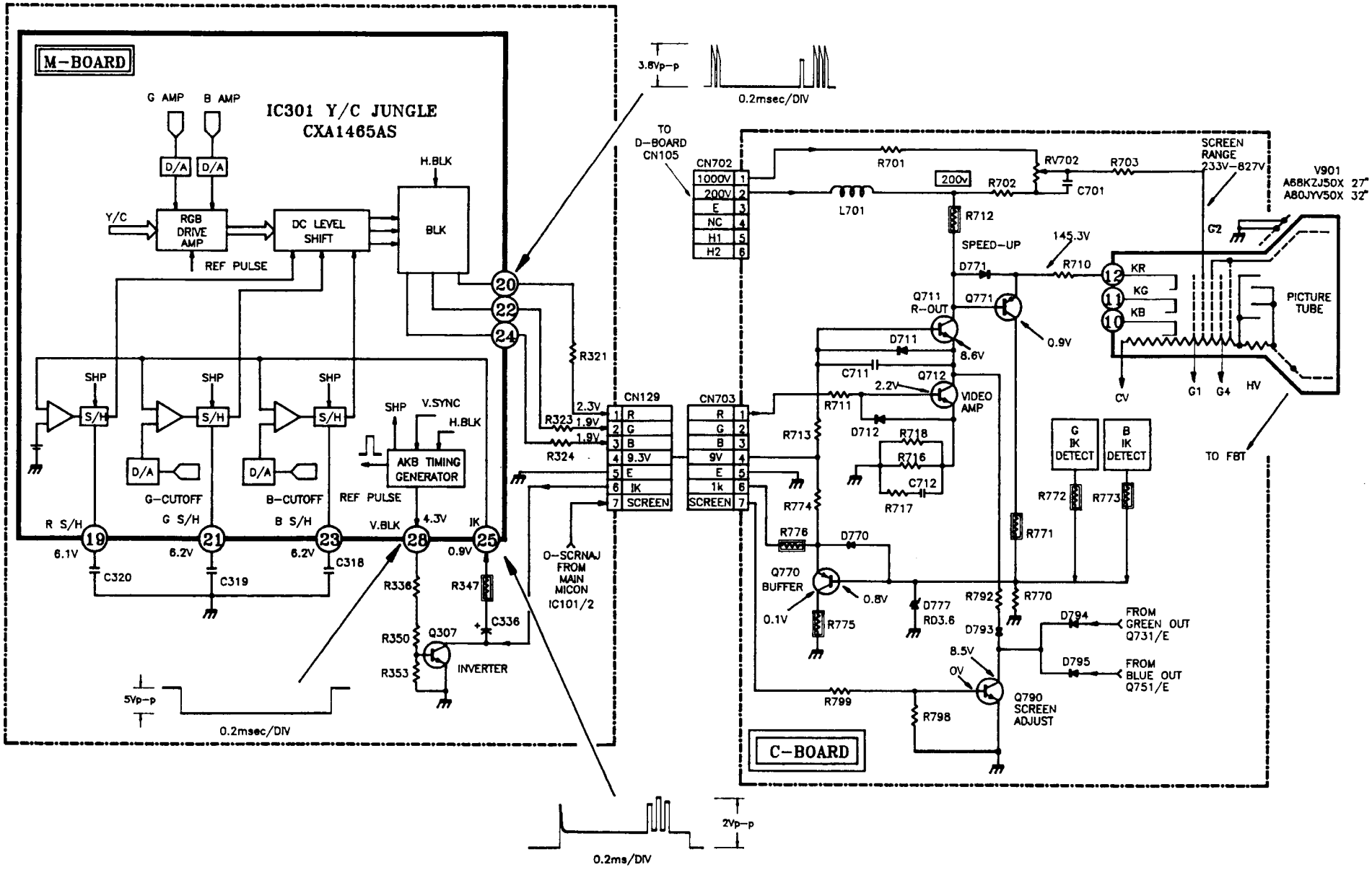


AUTOMATIC CATHODE BIAS

AKB Troubleshooting

When servicing for problems with the video information, especially no raster conditions, you should confirm proper operation of the AKB circuitry. You can do this by observing the voltages present at the Y/C jungle IC301 pin 19 (R-S/H), pin 21(G-S/H) and pin 23 (B-S/H). Any voltage at these pins that measures considerably lower or higher than shown in the service manual is a good indication that a particular Red, Green or Blue drive section should be checked for possible defects. Also, monitoring for the presence of 2Vp-p AKB reference pulses at IC301 pin 25 (IK) and for 3.8Vp-p AKB reference pulses at IC301 pin 20 (Red Out), pin 22 (Green Out) and pin 23 (Blue Out) is required. Remember to synchronize the oscilloscope at the vertical scan rate using IC301 pin 28 (V.Blk) for a trigger signal to look at the AKB pulses.

For servicing purposes you can verify the integrity of the video section, within the Y/C jungle IC, by connecting an external 3Vdc source through an isolation resistor (1k ohms) at the junction of R347 and C336. These components can be found at IC301 pin 25 (IK). This procedure will produce a dim raster sufficient for troubleshooting.



AUTOMATIC CATHODE BIAS

Y/C Jungle / Main Micon Interface

The below diagram shows the many circuit interface connections between the main micon, IC101, and the Y/C jungle, IC301. As already explained, IC101 controls the operation of the peripheral ICs through I^2C bus addressing. Some examples are:

- To trigger vertical output drive, from the Y/C jungle IC301 pin 31.
- PIP switching.
- A/V switching.

The Y/C jungle, IC301, on the other hand monitors the various circuits, it controls, to determine their normal circuit operation. For instance, automatic cathode bias (AKB) operation, vertical sweep loss (filter) circuit found in the BA-1 chassis, and ABL are constantly monitored to detect circuit misoperation. From this loop the Y/C jungle, IC301, can trigger a no raster condition to protect the CRT. It is therefore important to understand the interface between these two ICs to be able to effectively troubleshoot the set.

Operation

Standby 5 volts is applied to the main micon, IC101, at pins 64 and 63. Reset to the IC is applied at pin 36. The system is generated by the external crystal, X001, connected to pins 34 and 35. The I^2C bus, for communicating with the Y/C jungle and the set's peripheral ICs, is at pins 53 and 55. Note however, IC101 communicates with the memory IC, in the I^2C format, from pins 54 and 56.

IC101 outputs data and clock signals to the Y/C jungle to trigger the Y/C jungle IC into operation. On the other hand, the main micon IC relies on the V pulse signal input to pin 48, from the y/c jungle IC301 pin 29 and the H pulse signal input to pin 47, from the flyback transformer, to generate on screen characters and the menu display. IC101 also relies on the H Sync detect signal, input to pin 28 (not shown), to capture all active stations during the channel preset menu select function.

During normal operation, the Y/C jungle IC outputs the following signals:

- V. drive, from pin 31, to the vertical output IC501 on the D board.
- R,G,B from pins 20, 22 and 24.
- V. BLK signal from pin 28.

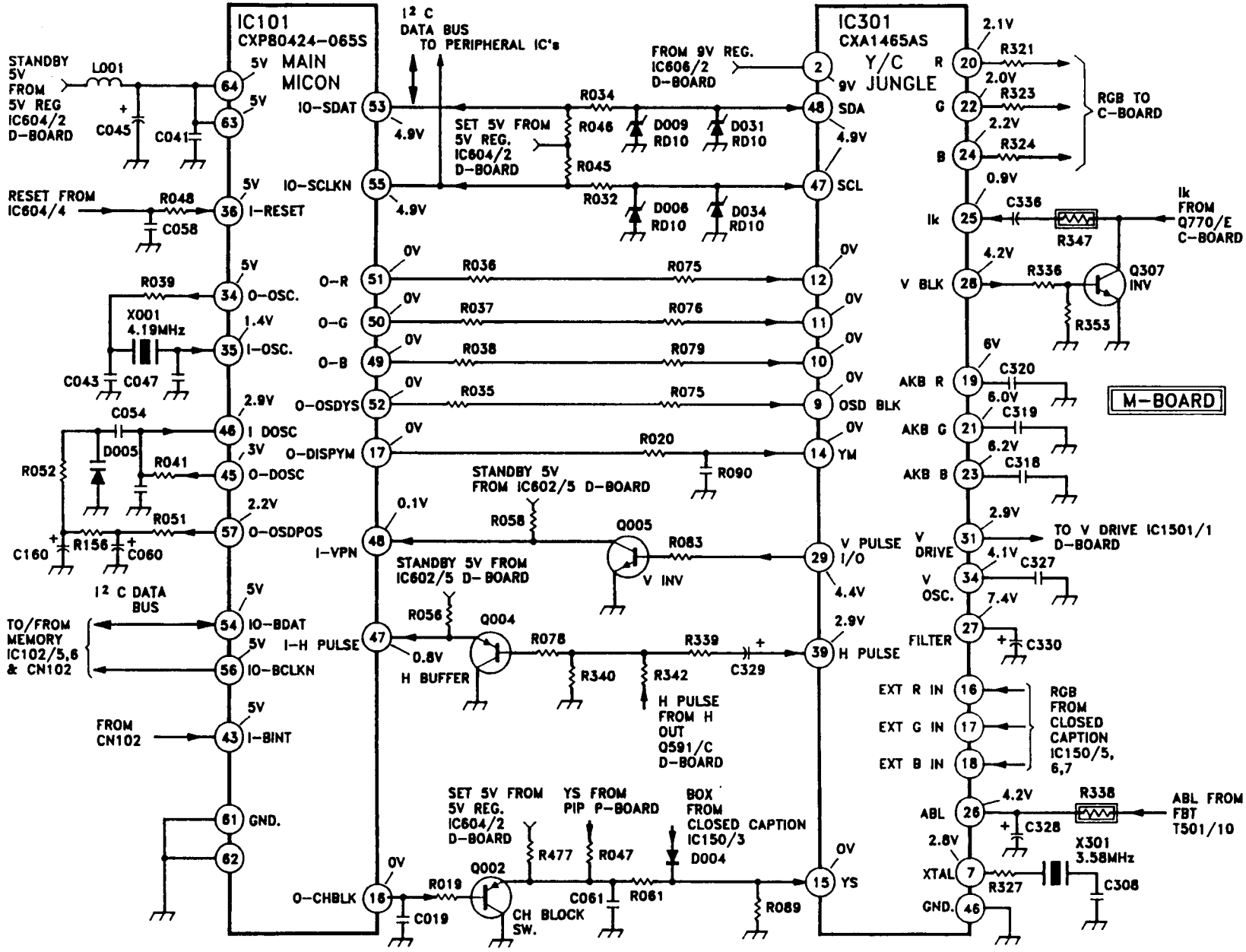
IC 301 will then check the following for normal operation:

- IK return pulses at pin 25 from Q770 emitter on the C board.
- AKB R, G, B reference voltages, at pins 19, 21, 23, generated from its internal sampling circuits.
- Filter, at pin 27, to detect the loss of vertical deflection (BA-1 chassis only).
- ABL, at pin 26, to limit the CRT's beam current and to detect hi-anode current overloads.

To generate on screen characters, IC101 utilizes an LC voltage controlled oscillator circuit connected to pins 46 and 45. IC101 can vary the voltage controlled oscillator frequency, to adjust the position of the display, from its pin 57 port. To do this, IC101 outputs a dc voltage to varicap, D005, through R051, R156, R052, C160 and C060 filter network. While in the service mode, this voltage can be changed by altering the data contained in the set's service register 34 to adjust the horizontal position of the on screen menu display.

The main micon outputs the RGB on screen character display signal from pins 51, 50, and 49 to the Y/C jungle pins 12, 11, and 10. It also outputs the blanking signal for the on screen display from pin 52 to the Y/C jungle pin 9. In order to synchronized the on screen character display, the main micon uses the V pulse and H pulse signals from IC301 pins 29 and 39 respectively.

IC101 outputs a DISPYM signal, from pin 17, to the Y/C jungle pin 14 to reduce the brightness of the main picture when the main menu palette display is being generated. X301, connected to IC301 pin 7, is used to generate the main color picture. The YS signal, input to IC301 pin 15 from IC101, is used to switch the closed - caption RGB signals into the main picture. The BINT signal, input to IC101, is used to download the set's initial service data to the main micon from an external computer.



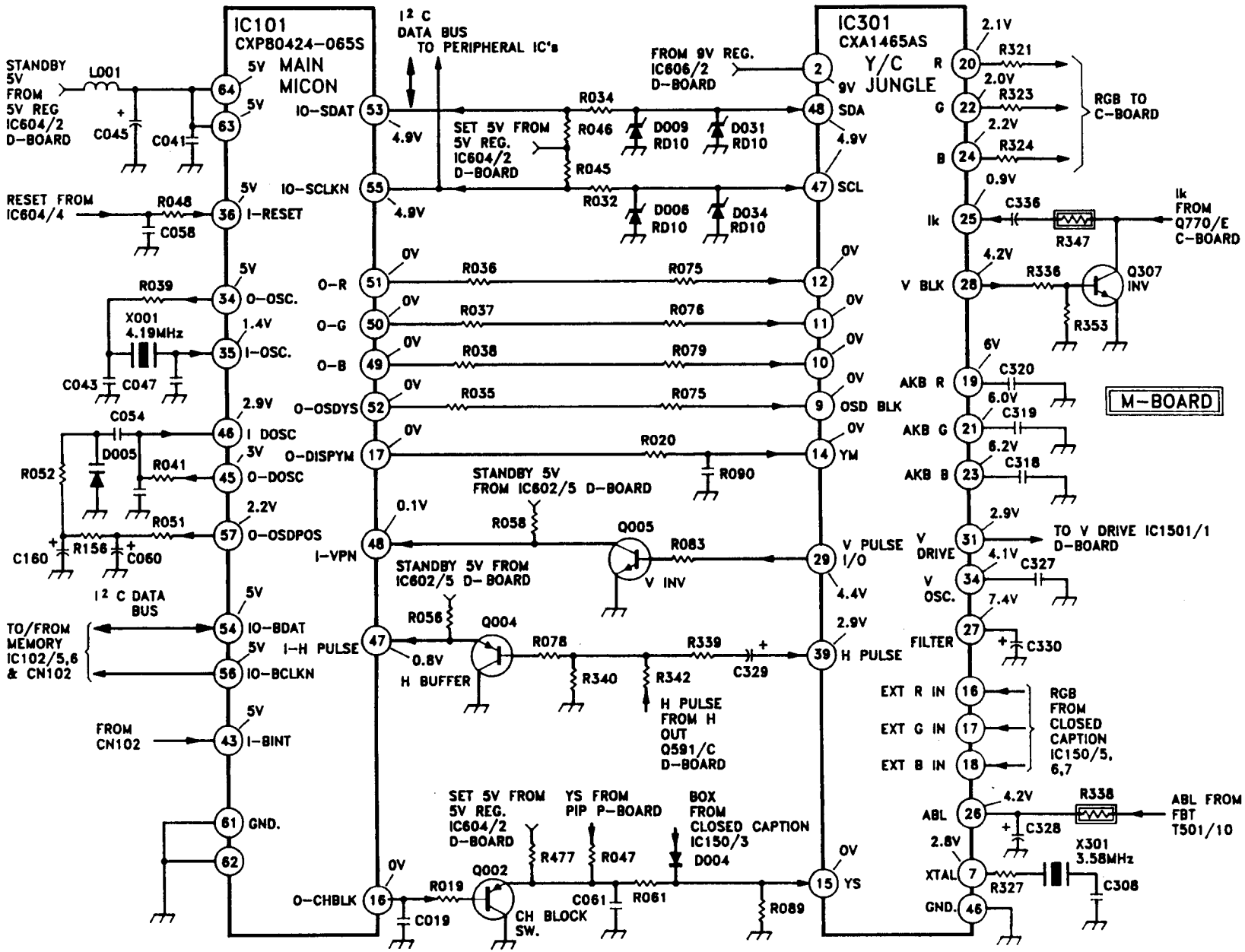
Y/C JUNGLE / MAIN MICON INTERFACE

Troubleshooting

Below is a list of strategic checks that you can do to troubleshoot no raster symptoms:

While servicing for no picture problems you should first determine if the problem is from loss of high voltage. You can do this quickly by checking the following:

- Look at the CRT filaments to see if they are lit. If the filaments are lit, it is a good indication that the power supply sections are functioning properly.
- Check the Y/C jungle IC301 pins 20, 22, and 24 for RGB outputs
- Turn up G2 to see if there is raster. If there is raster, it is a good indication that the deflection circuits are functioning properly.
- If a horizontal line is displayed when turning up G2, then you should check for vertical output drive at IC301 pin 31.
- If vertical drive is missing then check for the presence of data and clock activity at IC301 pins 53 and 55. Without data or clock, IC301 cannot output a vertical drive signal however, the vertical oscillator will function.
- If vertical drive is present, you should check IC301 pin 27 for 7.7Vdc. If this voltage is missing or LOW (1.2Vdc) then check the following:
- Vertical deflection IC501 pin 3 for flyback pulses.
- Check also the vertical sweep loss transistor, Q314, for PN junction failure.
- Check IC301 pin 26 (ABL) for 7.4Vdc. If less than 7.4Vdc, then check the components around the flyback T500 pin 10 for failure and suspect the flyback.
- Check the operation of the AKB circuits for the following:
- IC301 pins 20, 22, and 24 for IK (cathode current) set up pulses.
- Check for AKB return pulses at IC301 pin 25.
- Check IC301 pins 19, 21, and 23 for more than 4.2Vdc.
- Check IC301 pin 14 for a LOW (0Vdc) especially if characters are displayed with no raster. If a HIGH (5Vdc) is present, it is a good indication that the closed - caption picture circuitry may be triggered. You should check the appropriate switching for the closed - caption circuitry.



Y/C JUNGLE / MAIN MICON INTERFACE

Closed - Caption Format

The closed - captioning system provides for the transmission of caption information and other text material. This information is transmitted as an encoded composite data signal during the unblanked line 21, in field 1 of the NTSC video signal. A framing code is also transmitted during the unblanked line 21, in field 2. The NTSC composite video signal waveform, for both odd and even fields, is illustrated in figure A below.

The encoded closed - caption signal, contained within the active portion of line 21, consists of a 0.503MHz 7 cycle lead-in signal, a start bit, and 16 bits of data. This waveform is illustrated in figure B below.

The 16 bits of data consists of two alphanumeric characters patterned to the USA Standard Code for Information Interchange (USAA-1SCII) format. This is illustrated in figure C below. The closed - caption characters are normally displayed in white (may also be displayed in color) on a black background.

The line 21 closed - captioning system allows four different data channels to be multiplexed within the line 21 data stream. The start of a particular channel data stream is identified by a unique command code. Once a unique command code is received, all subsequent data is considered to belong to that data channel, until another unique command code is received by the decoder. The four types of captions possible are labeled as follows:

- Language (C1), and Language (C2) captions. This is the actual program material transmitted in script from.

Captions is defined as video related information, however, its display is not allowed to fill the screen. Captions may be displayed anywhere on the screen limited to four rows displayed at any one time. The closed - caption video information may be displayed in two ways: roll-up or pop-on.

Roll-up

In the roll-up mode, captions are displayed in two, three or four consecutive rows. Data appears in the base row and scrolls up as new information is received. In other words, the top row of caption information scrolls OFF the screen and the new information comes in from the bottom.

Pop-on

In the pop-on mode, two display memory ICs are utilized to exchange data information. In this mode one memory displays the current text while the other memory accumulates the text to be displayed next. A special command signal is then sent to exchange the information contained in the two memories, thereby causing the entire caption data to appear at once.

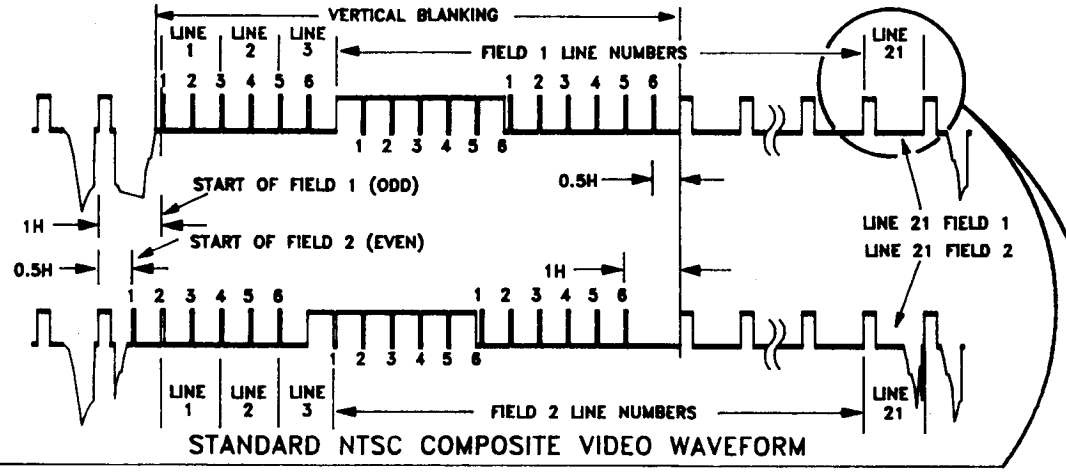
The AA-1 and BA-1 chassis closed-captioning decoder IC functions in the roll-up when set to the CC-1 decode mode and in pop-on when set to the CC-2 decode mode.

- Language (T1), and Language (T2) text captions. Text captions is information generated solely for the purpose of informing the viewer of the station's hourly programming.

Text

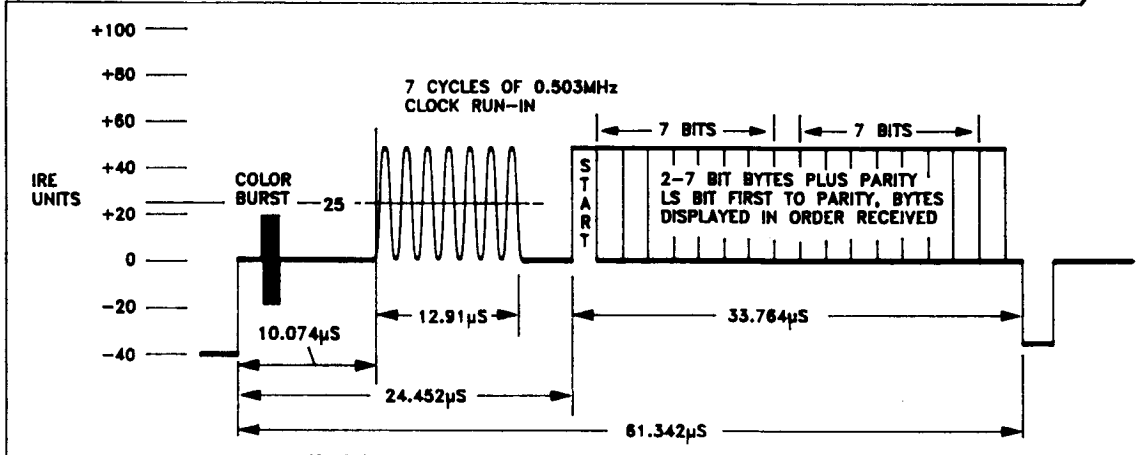
Text is defined as non-video related information, so its display can fill the screen. In this mode, a black box 8 rows high by 34 columns wide covers the screen. Then text is displayed from the top to fill a maximum of 8 rows. When all 8 rows are filled, the display scrolls up as new information is received.

FIG.A



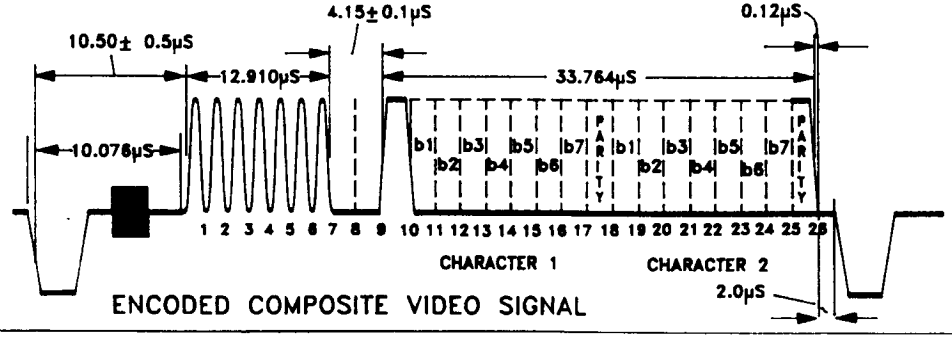
STANDARD NTSC COMPOSITE VIDEO WAVEFORM

FIG.B



LINE 21 CLOSED-CAPTION VIDEO SIGNAL

FIG.C



ENCODED COMPOSITE VIDEO SIGNAL

EXPANDED VIEW OF LINE 21

CLOSED - CAPTION FORMAT

Closed - Caption Decoder

The closed - caption decoder IC functions to display the closed - caption transmissions conforming to the line 21 NTSC format. To display this information, the closed - caption decoder IC requires a closed - caption encoded NTSC composite video signal, a horizontal sync signal, and an external keying circuit to trigger the closed - caption video output. The closed - caption decoder IC can display up to 8 rows of 32 columns ASCII characters (utilizing an on board RAM chip ASCII character set) over a black graphics box anywhere on the screen.

Operation

The AA-1 chassis utilizes Motorola's closed - caption decoder IC for decoding the line 21 NTSC closed - caption signal. A pin compatible Zilog closed - decoder IC is used in the BA-1 chassis TV sets. Both ICs function in the same manner, therefore the circuit description here applies to the operation of the Zilog IC as well.

Set 5Vdc is applied to IC150 pins 14, and 15 from the set 5 volts supply IC602 pin 5. Reset is applied to the IC through R150, at pin 2 from the reset IC602 pin 4. IC150 pin 16 sets the control functions of pins 1, 17, and 18 within the IC. When set to 5 volts pins 1, 17, and 18 perform the control functions of decoder ON/OFF, caption/text, and language 1/language 2 select respectively. The IC functions in the following manner:

The composite video signal is coupled from the comb filter through R301, buffer Q301, R158, buffer Q151, C157, and R154 to IC150 pin 11. Within the IC the composite video signal is processed to RGB information and output from pins 5, 6, and 7. To trigger RGB outputs, from the IC, the closed caption decoder IC relies on the following:

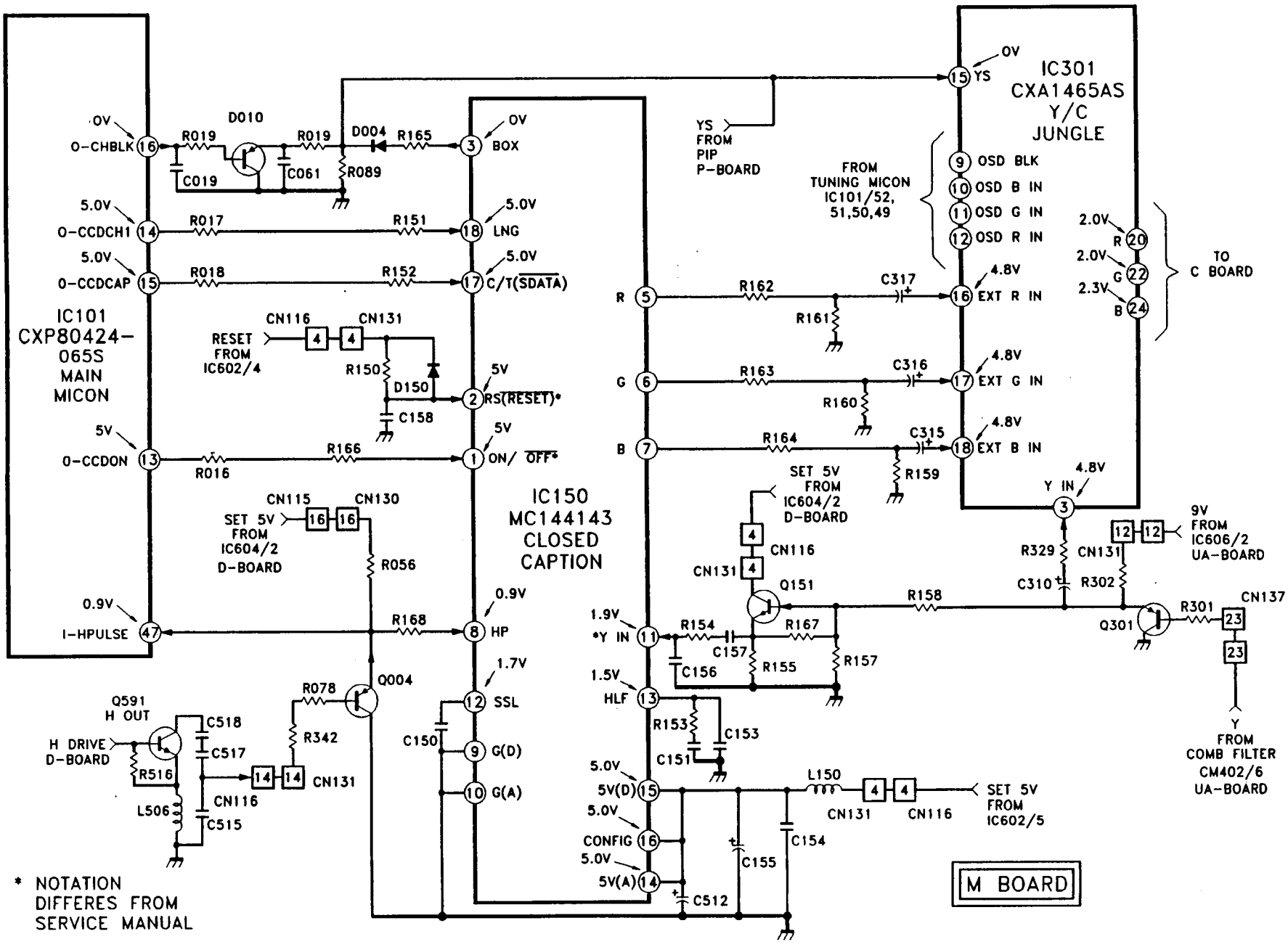
- The HP pulse is coupled from the horizontal drive output transistor, Q591, through R342, R078, buffer Q004, and R168 to pin 8. Without the HP pulse, the closed caption decoder IC cannot process or output the closed caption data input to pin 11.
- A HIGH (5Vdc), output from IC101 pin 13 to IC150 pin 1, to enable the IC.

Following these inputs, closed-captions or text data, are output from the IC based on the logic level of the decoder IC150 pin 17 and pin 18. The tables below show the CMOS logic levels for pins 17 and 18.

IC150 pin 17 CMOS logic level	
HIGH	Captions are processed
LOW	Text is processed

IC150 pin 18 CMOS logic level	
HIGH	Language (1) is processed
LOW	Language (2) is processed

To switch the closed-caption RGB data, output from IC150 pins 5, 6, and 7 into the main picture, the decoder IC150 pin 3 outputs CMOS level signals to the Y/C jungle IC301 at pin 15.

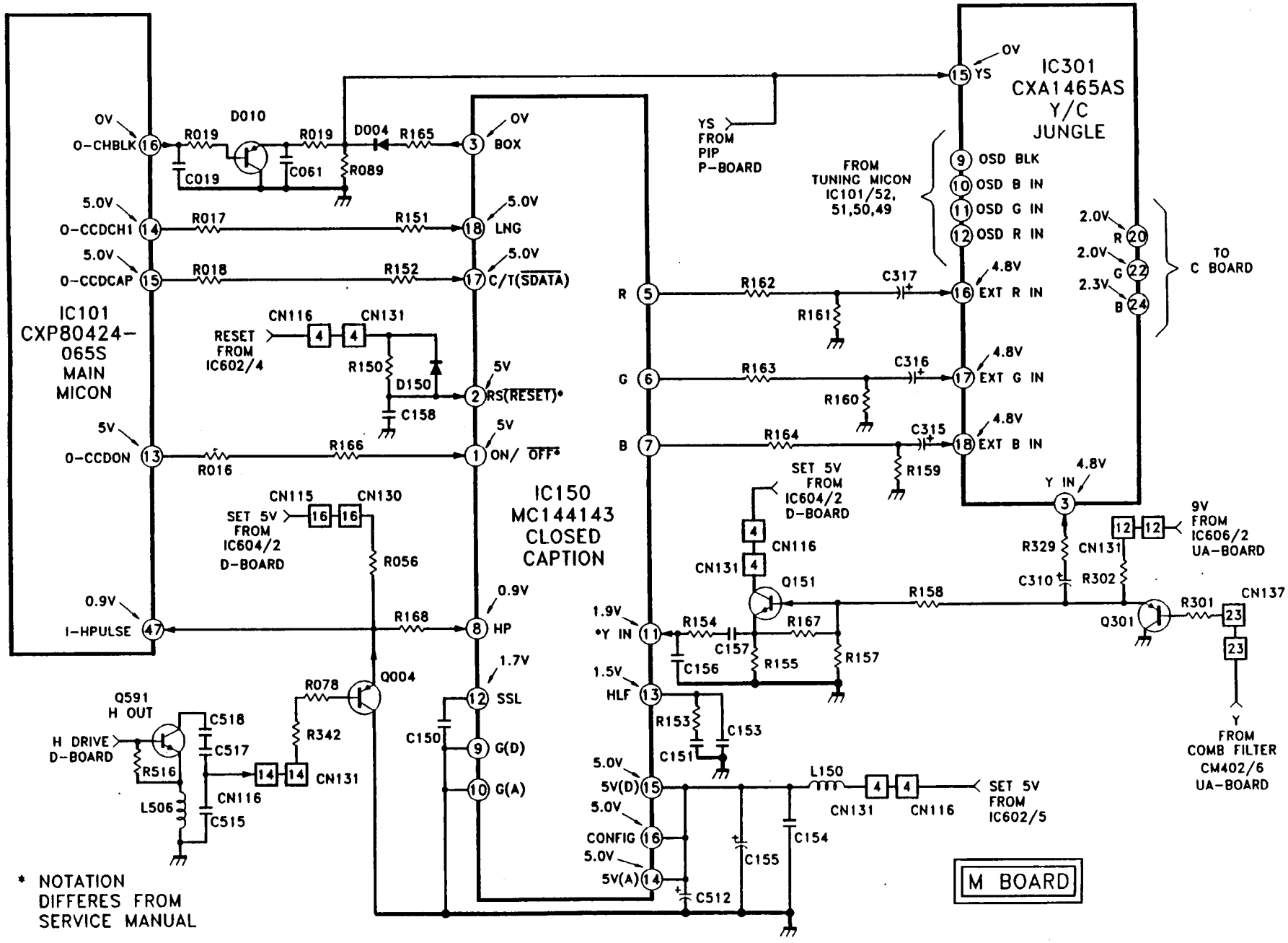


CLOSED - CAPTION DECODER

Troubleshooting

To output caption information, the IC must receive a video signal that has the closed-caption data. To verify this do the following:

- Check Vcc, reset and ground.
- Playback a tape known to contain closed captions.
- Verify that there is a video signal being input to the decoder IC150 at pin 11.
- Verify IC150 pin 1 is 5Vdc. This enables the IC to decode the video signal input to pin 11. If it is 0Vdc, select menu on the remote control and verify caption, (CC1), is turned ON. (Refer also to the tables in the previous page for the pin 17 and pin 18 voltages to ensure the decoder is set to the CC1 language mode).
- Verify that there is an HP signal present at IC150 pin 8. Without the HP signal there can be no decoding of the closed caption signal.
- Verify there is a digital signal output from IC150 pin 3 to the Y/C jungle IC301 pin 15. When closed captions are being decoded, the decoder IC outputs the YS signal to allow the closed caption RGB data to be switched into the main picture.
- Verify also that there is RGB outputs from decoder IC150 pins 5, 6, and 7 to the Y/C jungle IC301 pins 16, 17, and 18.



CLOSED - CAPTION DECODER

Picture-In-Picture

The picture in picture feature is available on the AA-1 chassis and is located on the P board. The picture in picture function is controlled by the main micon through data on the I^2C bus. The storage of the child picture and the creation of the picture insert is controlled by the PIP CONTROL IC3201. 4 ICs are used to do this:

- The PIP Analog Process IC3204 is responsible for the switching of the main and child picture as well as producing the chroma sync signals.
- C A/D-D/A IC3202 converts the child picture chroma from the PIP ANALOG SWITCH for storage by the PIP control.
- Y A/D-D/A IC3203 converts the child picture Y signal from the A/V switch IC402 (on the UA board) for storage by the PIP control.
- The MEMORY IC3200 is used to store the child picture in PIP mode.

The P board is necessary for normal television operation. Without it there will be no picture, however, there will be an on screen display and closed caption information. The PIP circuit is described below in two modes of operation; normal picture and PIP mode.

Normal Picture Operation

During normal operation the chroma and luminance signals for the main picture will be looped through the PIP Analog Process, IC3204, as follows:

Chroma - The chroma signal is input at pin 39 (C IN) and is switched to pin 41 (C OUT) where it will be .7Vp-p. The main chroma signal is also internally applied to an oscillator circuit to provide chroma sync for the child picture. The chroma signal is amplified to 1.3Vp-p and buffered and applied to the Y/C jungle IC301 pin 5 on the M board (not shown).

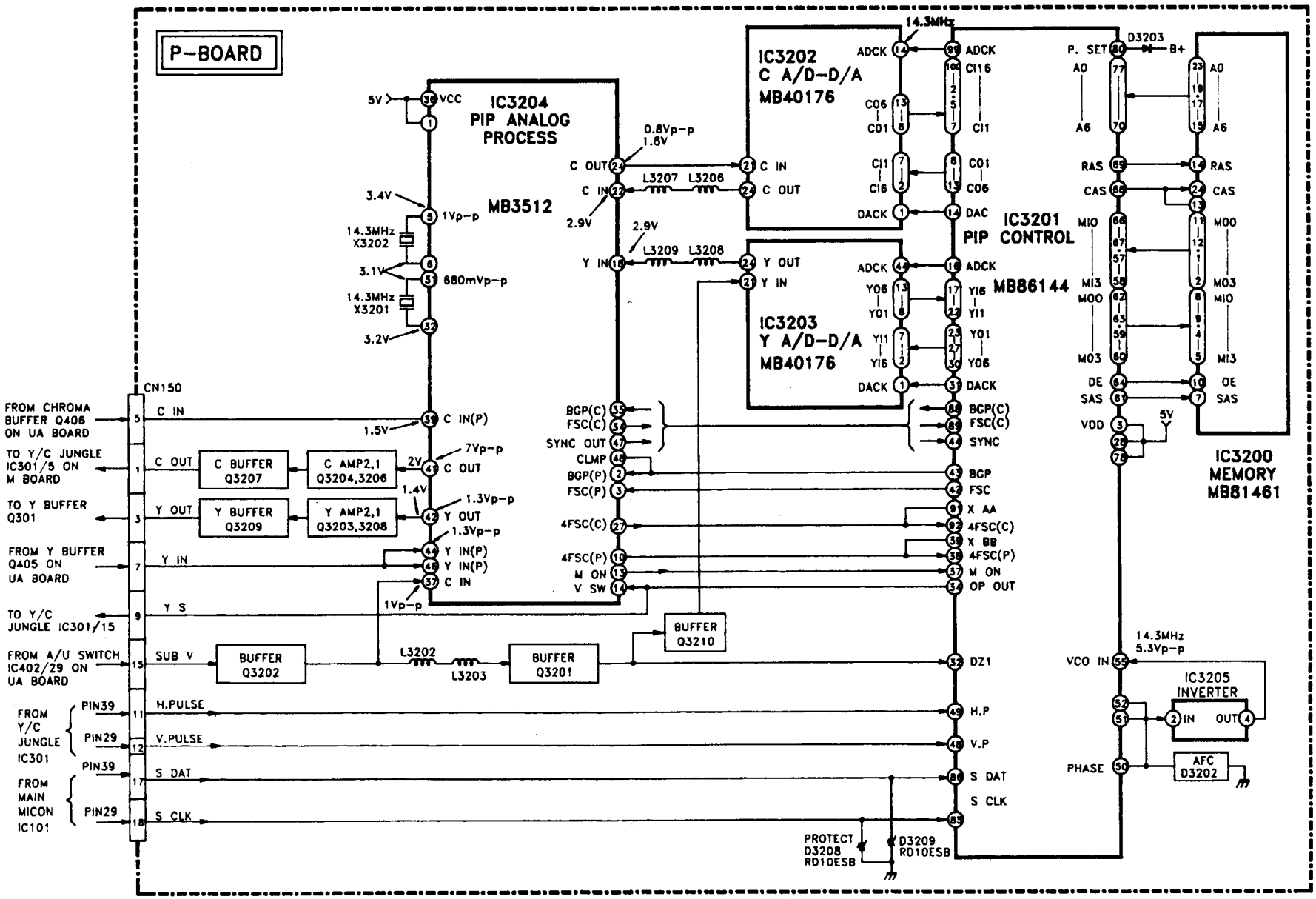
Luminance - The luminance signal is input at pin 44 (Y IN) and is switched to pin 42 (Y OUT) where it will be 1.3Vp-p. The Y signal is amplified to 2.5Vp-p , buffered and applied to the Y/C jungle IC301 pin 3 (not shown).

PIP Mode

When PIP mode is selected the A/V switch IC402 (not shown) will select the child picture signal and output it at pin 29. This composite video signal is separated into Y and C signals on the P board.

Chroma - The chroma signal is applied to the PIP ANALOG SWITCH IC3204 pin 37 (C IN). The chroma signal is switched internally and output at pin 24 (C OUT) where it is applied to the D/A converter IC3202 pin 21. The .8Vp-p chroma signal will then be processed by the PIP control and cycled through the memory IC3200. The memory IC is always processing information.

Luminance - The Y signal for the child picture is separated by L3202 and L3203, buffered and applied to the D/A IC3203 pin 21(Y IN). The 2.9Vp-p Y signal is then digitized and processed by the PIP control and cycled through the memory IC3200.



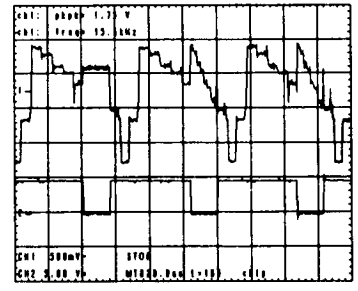
PICTURE-IN-PICTURE

Insertion of Child Picture

The PIP controller is responsible for inserting the child picture into the main picture. It does this by replacing the main picture with the child picture at a predetermined location. The box which the child picture fits into, is switched in and out by switching pulses produced by the PIP control. This signal is labeled V SW (pin 14) on the PIP analog process IC and OP OUT on the PIP control. The switching pulses appear as a packet at the field rate. There will be one packet present for each field. The following oscillograph shows the relationship between a field of video and the switching pulses.

Top - field of video (500mV/div)
Bottom - V SW pulses (2V/div) T.B - 2ms

If a digital scope were used to observe this waveform, the exact line number could be scaled in to examine the child picture line by line. The following oscillograph shows the Y signal of lines 165-167. The child picture is inserted when the V SW pulse goes LOW. If this signal stays LOW, the main picture will appear black. If this signal stays HIGH, the child picture will appear as a semi-transparent window.



Top - CN150 pin 3 (Y OUT) 500mV/div
Bottom - V SW (IC3204 pin 14) 5V/div 20usec/div

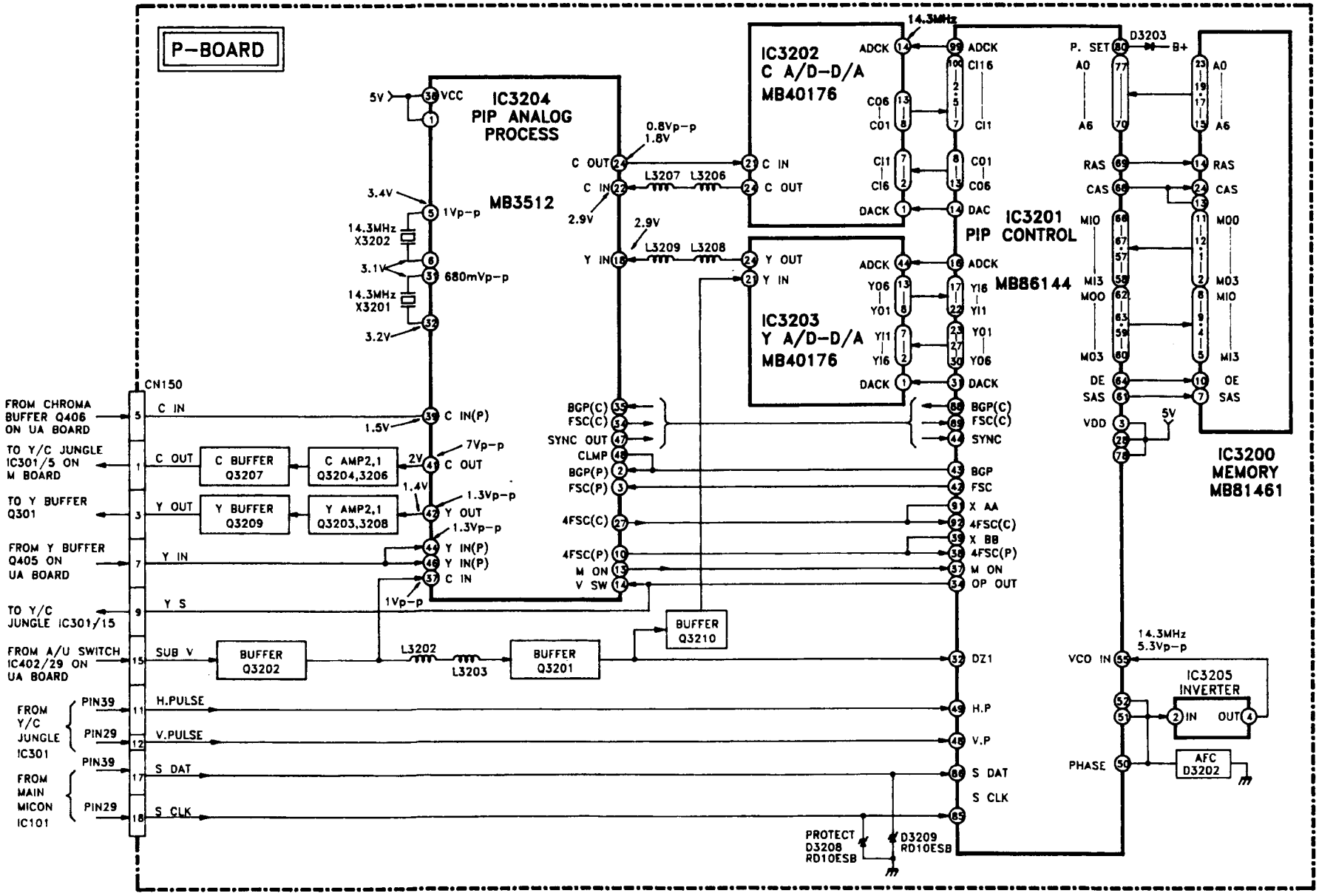
The phase and timing of the V SW pulse is determined by the 14.3MHz 4Fsc signal from the PIP analog process IC3204 pins 27 (4FSC[C]) and 10 (4FSC[P]). If there is no parent picture, the child picture will lose its chroma reference and therefore appear in black and white.

Troubleshooting PIP

The first step in troubleshooting the PIP section is to verify the "must-haves". In this case, they are as follows:

1. 5Vdc to all ICs.
2. I^2C data and clock to IC3201 pins 86 (SDAT) and 85.
3. 4.3MHz at IC3204 pins 5,6 (X3202) and pins 31,32 (X3201). See diagram below for voltages.
4. The V SW switch pulse (IC3204 pin 14) should be HIGH during normal mode.
5. 5.3Vp-p, 14.3MHz at IC3201 pin 55 (VCO IN).

If any of these are missing, troubleshoot that area before proceeding.



PICTURE-IN-PICTURE

Defective Child Picture

If the child picture should be defective ie; no color, mosaic effect, the following should be checked.

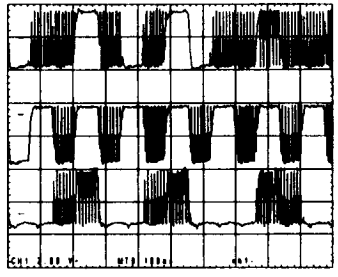
1. Chroma signal at IC3204/ pins 24 (C OUT) and 22 (C IN).

2. Y signal at IC3204 pin 18 (Y IN).

3. Digital data on all data lines between the D/A converters (IC3202 and 3203) and the PIP control IC3201.

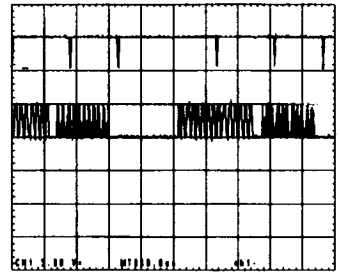
4. Digital data between the control IC3201 and the memory IC3200 at all times.

The output enable line from IC3201 pin 64 (OE) will always have activity on it. You should see a change in activity level when you freeze the picture. If the picture does not freeze, ground the OE line to freeze the picture. If the picture freezes, the PIP control is defective. The following oscillograph shows the data lines from the D/A converter IC3202.

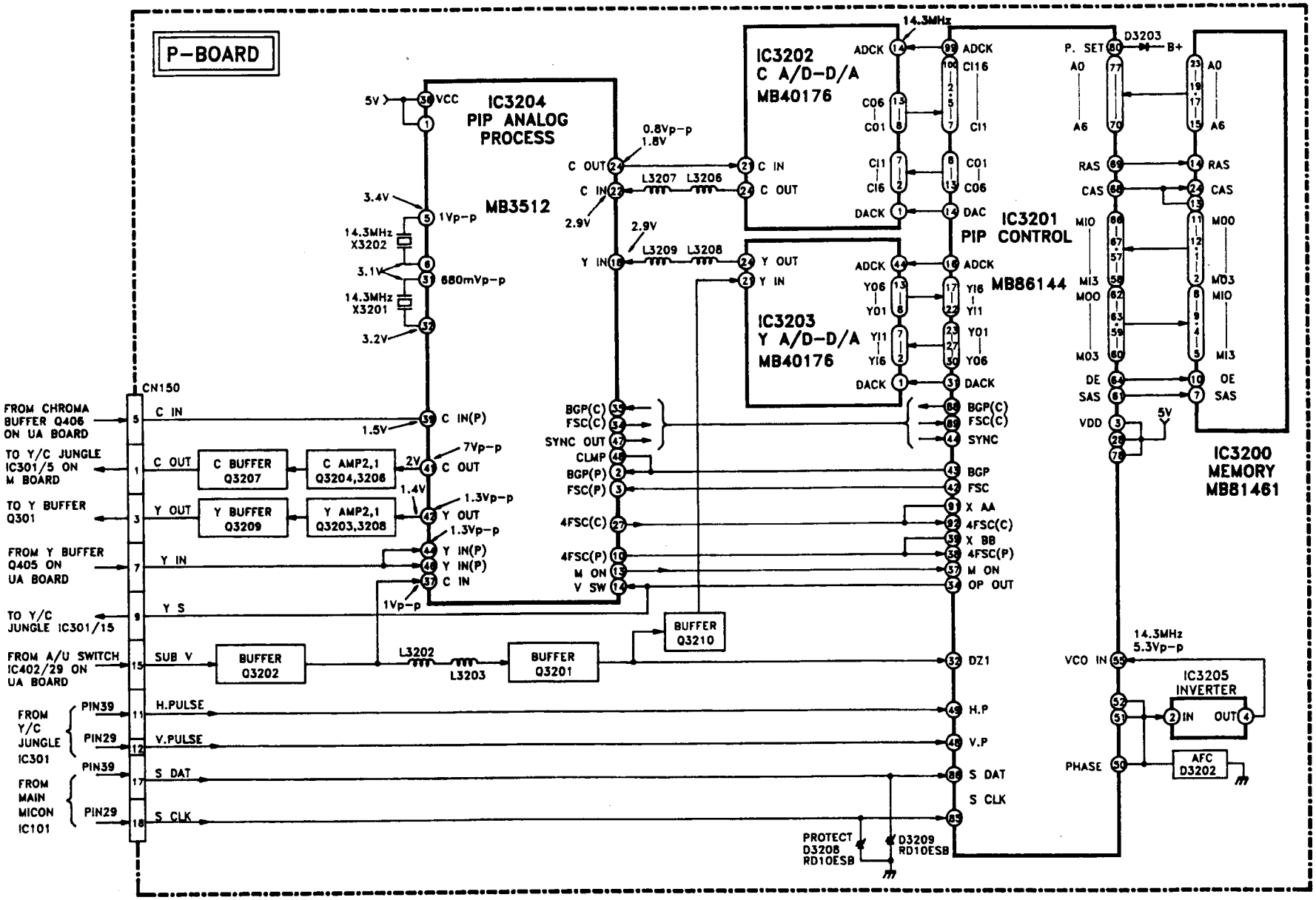


Top - IC3202 pin 8
Middle - IC3202 pin 11
Bottom - IC3202 pin 13
Both waveforms are at 2V/div. and 100nsec/div.

The next oscillograph shows the output enable line (OE) and the serial address signal (SAS) from the PIP control IC3201 pins 64 (OE) and 61 (SAS). These lines should always be active.



Top - IC3201 pin 64 (OE)
Bottom - IC3201 pin 61 (SAS)
Both waveforms are at 2V/div. and 10usec/div.



PICTURE-IN-PICTURE

Dynamic Convergence

Overview

The Dynamic Convergence circuit is necessary due to the design of the CRT. In most CRTs the RGB electron guns are arranged in an "in-line" configuration. In this type of set-up, the distances the individual RGB electron beams have to travel to the center of the screen is equal. However, as the beam travels to the sides of the tube, the distance and angle each must travel is different. Since all three beams must arrive at the same spot at the same time, a dynamic convergence circuit is employed.

The dynamic convergence circuit develops corrective signals which are applied to a convergence yoke. The windings of this yoke are located on the back section of the deflection yoke. By varying the current through the convergence yoke, the dynamic landing of all three RGB electron beams can be controlled. To develop this drive signal, it is necessary to start with both horizontal and vertical signals. These signals are needed to synchronize the convergence signals generated within the waveform generator IC. The output signals from this IC are then mixed in the convergence circuit to generate the final convergence drive signal, which is applied to the convergence yoke.

H-STAT Control

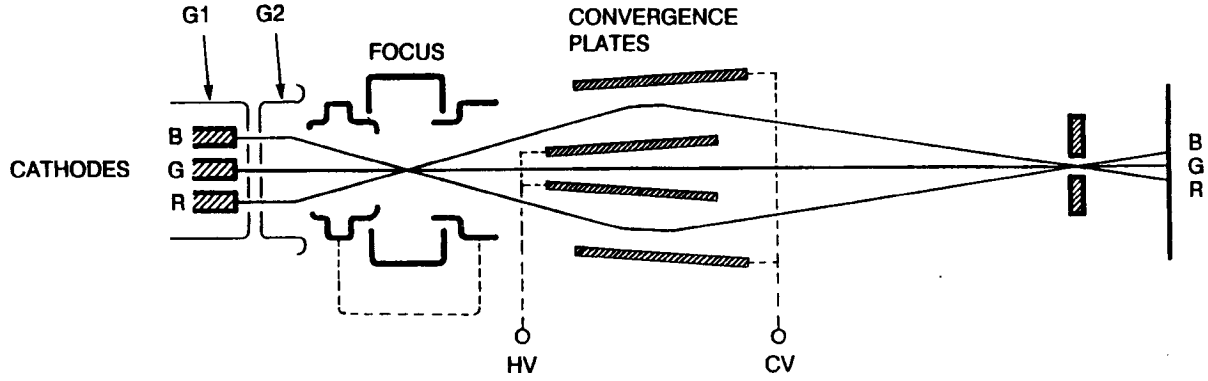
Sony's unique Trinitron CRT uses a one gun assembly, instead of the three gun assembly used in a conventional CRT. With a one gun assembly, it is necessary to provide a static convergence voltage to special plates in the neck of the CRT to provide center convergence. To accomplish this, an H.STAT control (not shown) is employed. This control varies a high voltage (slightly less than the HV applied to the second anode) to allow the three beams to converge in the middle of the tube.

To check for proper operation of this H.STAT control, use a crosshatch pattern. Using the pattern, if this voltage is missing or incorrect, the symptom is misconvergence. However, only the vertical lines of the pattern will separate into separate RGB vertical lines. Generally, the displacement of these lines will be even from top to bottom. If an H.STAT problem is suspected, adjust this control to determine if it is operational. If it is operational, check the dynamic convergence circuit.

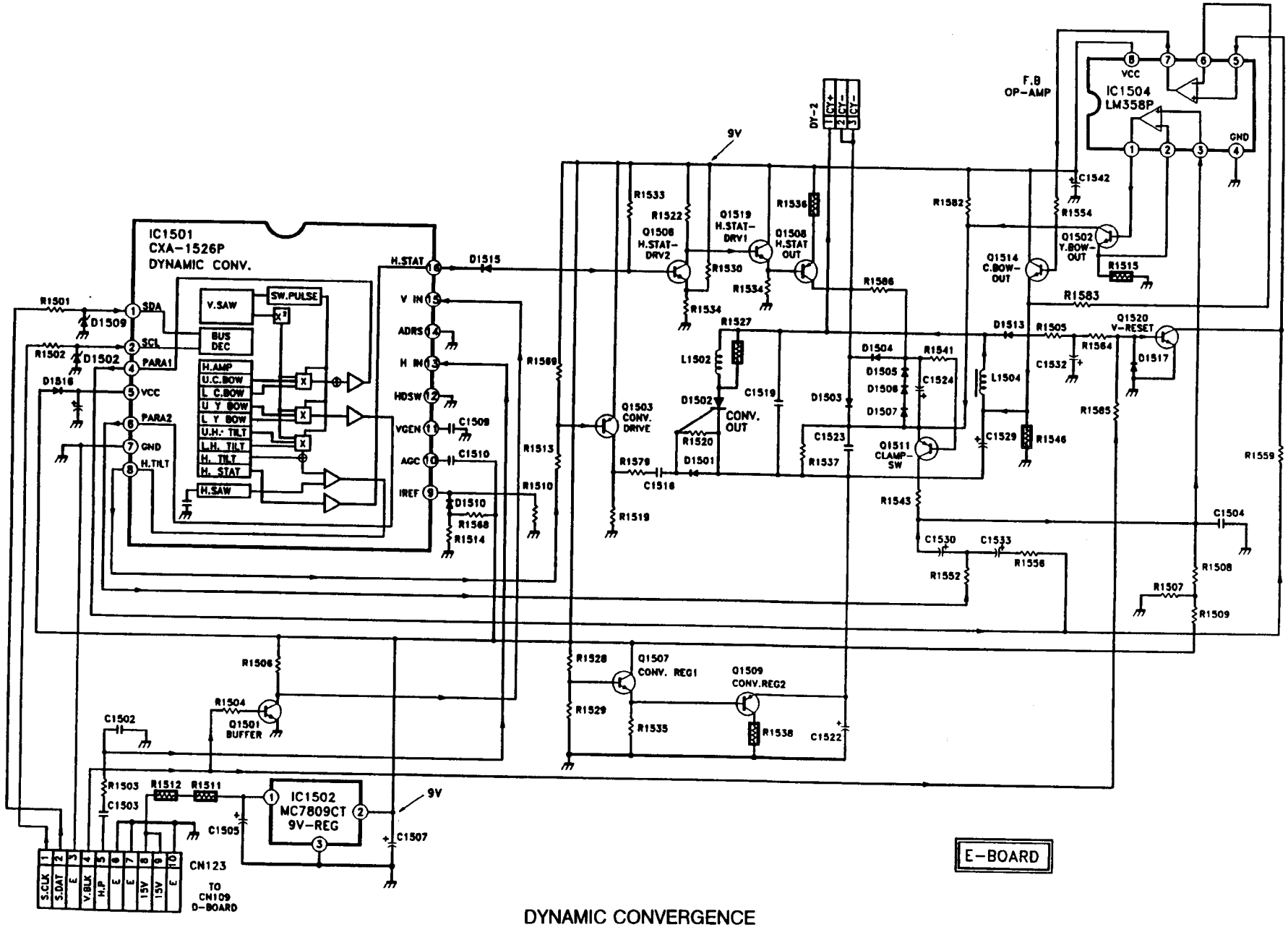
Support Signals and Main Output Signals of IC1501

The dynamic convergence circuit is located entirely on the D board. Also located on this board is the Velocity modulation circuit. These two circuits are almost totally independent of each other. The only connections between them is that they both need the H. pulse and the V. BLK signal. They use separate B+ lines.

A horizontal H. pulse and a V. BLK pulse from connector CN123 pins 5 and 4 respectively are applied to IC1501, the dynamic convergence waveform generator at pin 13 (horizontal) and pin 15 (vertical). The H. pulse is derived from the flyback transformer, T501, pin 9. The V. BLK is derived from the Y/C jungle, IC301, pin 2 on the M board.



CONVERGENCE FIGURE



DYNAMIC CONVERGENCE

These signals synchronize the waveforms generated by this IC. Inside the IC, the following horizontal and vertical waveforms and voltages are generated:

PIN No.	Name	Waveform
Pin 4	PARA 1	Vertical rate rounded sawtooth
Pin 6	PARA 2	Vertical rate inverted parabola
Pin 8	H.TILT	Horizontal rate square wave (60/40 duty cycle)
Pin 16	H.STAT	DC voltage, normally 3.6 Vdc (variable 2.5 - 7 Vdc)

To generate these output signals, the B+, data and clock signals are the input support signals applied to the E board via connector CN123 to these circuits:

Supply Voltage

15 Vdc is applied through connector CN123 pins 8 and 9, R1512 and R1511 to the 9 volt regulator, IC1502, on the E board.

Serial Data and Clock Pulses

There are no potentiometers used in this circuit. Adjustments to this IC are made through the I^2C data bus from the main micon IC101. This data is changed using the remote control unit when the set is put into the service mode. In the service mode, the data entered with the remote control is applied to the main micon IC101. This IC then applies it to IC1501 to control its internal registers. After each setting is adjusted, the setting must be saved into the EEPROM IC102 by a Write command. The clock pulses are necessary for all transmission of data.

At power ON, the settings stored in the EEPROM are recalled by the main micon and applied to IC1501. This data sets the internal registers to produce the desired convergence adjustments. If this data line is open, thereby preventing this data from being applied to IC1501, the IC will cause misconvergence. The data from the main micon, IC101, is updated constantly so IC1501's data is also being refreshed. For example, if the data line was opened at power ON, the convergence will not be correct. However, if the data line is reconnected anytime thereafter, the data will be accepted by IC1501 and the convergence will be restored to the adjusted settings.

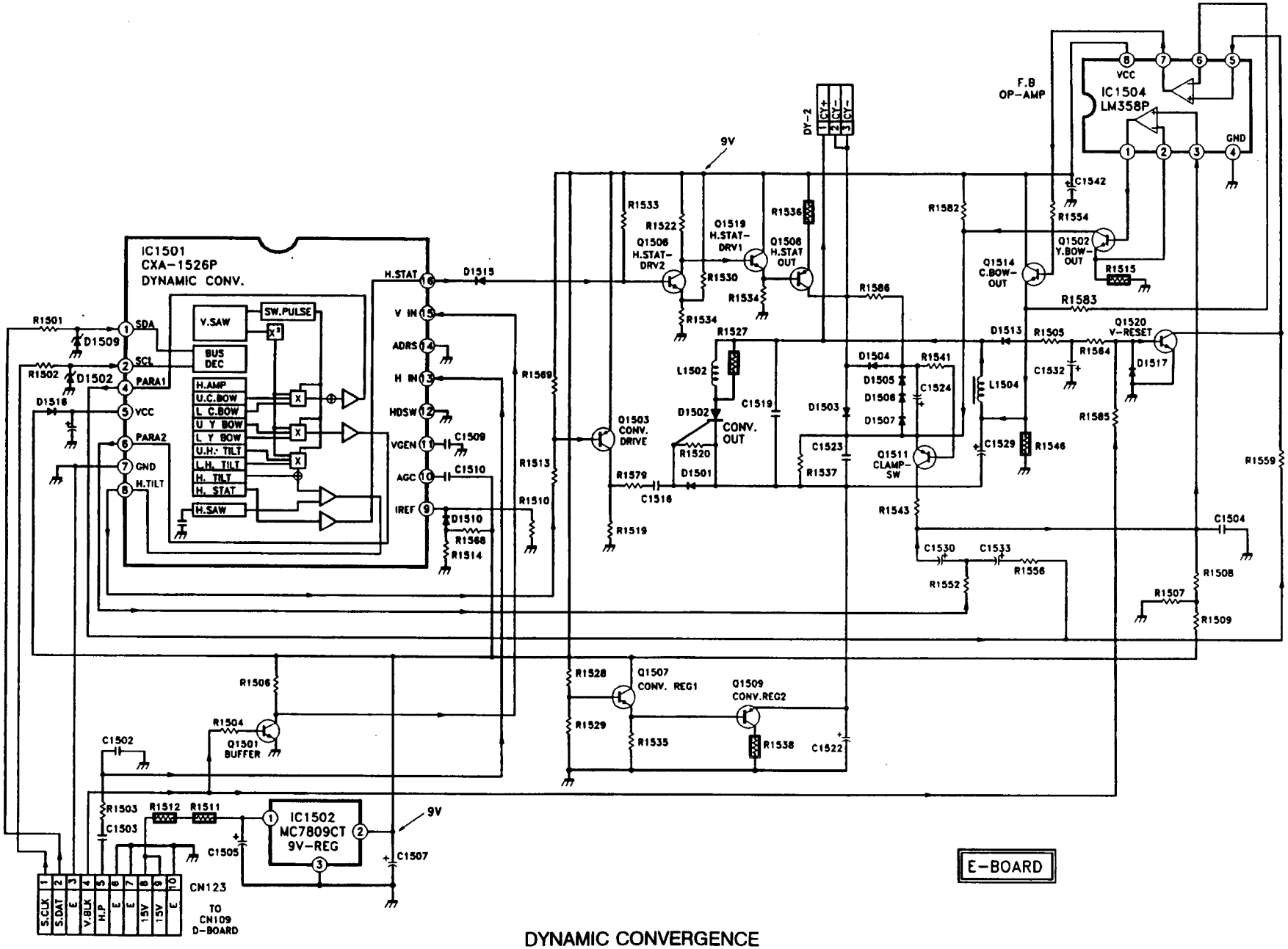
Circuit Operation

When the necessary support signals are applied to IC1501, it will output four signals. These are applied to the remainder of the convergence circuit to produce the final dynamic convergence signal applied to the convergence yoke. For simplification, the processing of these four signals will be explained separately until they mix together.

- The vertical rate parabola signal from IC1501 pin 6 (Para 2) is applied through R1552 and C1530 to comparator IC1504 pin 3. The output at pin 1 is applied to the base of Q1502 (Y Bow Out). The signal from the emitter of Q1502 is applied to IC1504 pin 2 – the inverting input of the op amp. This configuration makes the op amp act as a buffer. The amplified signal from the collector of Q1502 is clamped by Q1511 and applied through limiting diodes D1507, D1506, D1505 and R1586 to the CY- yoke terminal. This signal will vary the CY- potential.

- The vertical rate sawtooth waveform from IC1501 pin 4 (Para 1) is applied through R1559 to IC1504 pin 5. The output signal from pin 7 is applied to the base of Q1514 (C BOW-OUT). The output from Q1514 emitter takes two paths. Path one is back to IC1504 pin 6, through R1586, which is the inverting input of the op amp. Due to the value of R1583 the op amp will supply some gain to the output signal. Path two is to ground through fuse resistor R1546. The voltage developed across R1546 is applied through L1504 to the CY+ terminal.

- The horizontal rate rectangular H TILT signal from IC1501 pin 8 is applied through R1513 to the base of Q1503 (CONV. DRIVE). The signal from the collector is coupled through R1579 and C1516 and is applied to the gate of SCR D1502 (Conv. Out). The SCR fires at the horizontal rate and is modulated by the vertical rate signal applied to the CY+ yoke terminal. From Q1514/E, this vertical signal is applied to the anode of the SCR through L1504 and the parallel network R1527 and L1502. A regulated B+ voltage (3Vdc) is applied to the cathode of SCR D1502. This voltage source is derived from converter regulators Q1507 and Q1509. This voltage determines the turn OFF point of the SCR. The SCR turns OFF when the modulated signal on the anode of SCR D1502 drops to or below the 3 Vdc, which is the level that is applied to its cathode. Therefore if the anode voltage increases, the CY+ yoke signal will decrease in amplitude and vice versa.



DYNAMIC CONVERGENCE

The final result of this process is to produce a modulated convergence waveform across the convergence yoke.

4. The H.STAT control at IC1501 pin 16 is a current sink pin. Its purpose is to control the voltage applied to the base of Q1506 (H.STAT DRV2) by dropping more or less voltage across R1533. The collector of Q1506 is applied to the base of Q1519 (H.STAT DRV1) to control the voltage at its emitter, which is connected to the base of Q1508.

H-Stat Out

The voltage at the collector of Q1508 is applied to the DY-2 pins 2, 3 (CY-) convergence yoke terminals to provide a dc offset voltage. This voltage is adjusted by varying the setting of the H.STAT adjustment. The effect of this dc offset is very similar to the regular main H.STAT control used to adjust the plates inside the CRT. When adjusted, the vertical lines divide into separate RGB lines.

Troubleshooting

To troubleshoot this circuit, first determine if there is a defect. Unplug the convergence yoke plug and check to see if the misconvergence change radically. Normally, the misconvergence should be equally spaced over 70% of the center picture area. Next, check the main H.STAT control located on the C board for proper operation, since it is more likely to fail. If it is determined that the convergence circuit is defective, the best way to troubleshoot it is through waveform analysis. With a scope, check the waveshape of the signal applied to the convergence yoke at both the CY+ and CY- terminals. If it is similar to the waveforms included in this section, most likely the circuit is operating normally. Also, check the dc level on both pins of the convergence yoke. If incorrect, check the dynamic convergence H.STAT adjustment (accessed in the service mode) and the components downstream of IC1501 pin 16.

If the signals applied to the CY yoke are abnormal, unplug the CY yoke and check the signals again. If the CY+ signal is more distorted, signal trace the PARA 1 signal and the H.TILT signals. The H.TILT signal should have a duty cycle of approximately 60/40. If the signal applied to the CY- is more distorted, signal trace the PARA 2 signal path.

IC1501 Pin Analysis

To aid in troubleshooting, the following signal analysis of IC1501 is provided:

Data and clock signals are applied to pins 1 and 2, respectively. If missing, IC1501 will operate abnormally, causing misconvergence. The CY+ signal on the convergence yoke distorts and collapses. The H.TILT signal on pin 8 duty cycle which is normally close to 60/40 increases to 90/10.

The PARA 1 and 2 signals from pins 4 and 6, respectively, will cause misconvergence and the convergence yoke waveforms to distort. To determine which is at fault, unplug the CY yoke, and scope the + and - sides. If the waveform on the + side is incorrect, the PARA 1 signal processing circuitry is at fault. If the waveform at the minus side of the yoke is incorrect, the PARA 2 signal processing is at fault.

If the H.TILT signal is missing, horizontal components in the CY yoke signal will be missing.

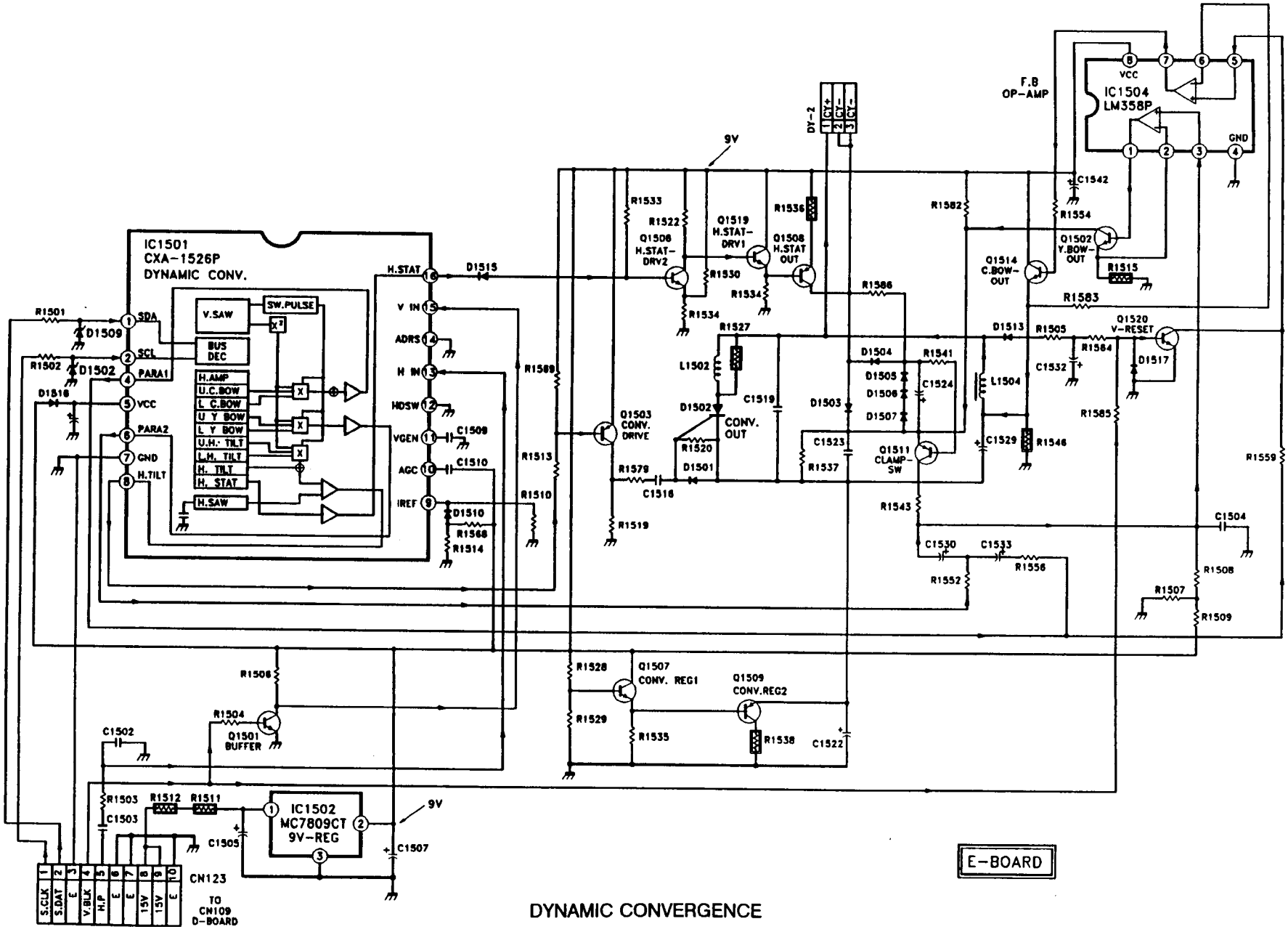
If either or both of the H IN (pin 13) or the V IN (pin 15) signals are missing, there will be no output waveforms from the IC, thereby causing misconvergence.

If internal the 1.9 Vdc I REF voltage at pin 9 is missing, misconvergence will result. IC1501 will not output any horizontal or vertical signals.

If the AGC pin is open (pin 10), the CY yoke signal will distort. If the pin is shorted, no vertical pulses will be output by the IC.

If the 9 Vdc is not applied to IC1501 pin 5, the IC will load down the data line. This will cause the set to either shutdown if it was operating or fail to come on if it was in the off position. If this condition is suspected, unplug the D board and check if the set can be powered up.

Note: When using the extender cables, stray signals may be picked-up by the cables which will affect the data line. This will cause erratic set operation. However, the convergence circuit can still be effectively analyzed.



DYNAMIC CONVERGENCE

I^2C Troubleshooting Tips

It is important to understand the sequence of events that occur when the unit is plugged in. This will help to troubleshoot various control problems.

Power Up Sequence

1. Plug unit in.
2. Reset. Housekeeping program runs.
3. Main micon polls EEPROM for last power and configuration info.

NOTE: The Main micon loads all customer settings and adjustment data into RAM:

- If power was last on, the main micon turns ON the power supply.
- If power was last off, Master does not proceed

d. When power command is issued by Master (either the set was last in the power on mode or the power button is pushed):

- Main micon turns ON the power supply.
- This in turn activates all the data switches.

NOTE: Vertical blanking is generated by the Jungle IC and fed back to the main micon for timing data transfer. This is a must have on ANU-1, ANU-2, AP, and FN-1 chassis only.

- Main micon loads from RAM all adjustment data to the slaves.
- Audio/Video muting is released.

This means that the main micon will poll the EEPROM for adjustment data only after reset. This can be verified by monitoring the DATA and CLOCK lines at ac plug-in. There should be a short burst of activity on the bus. If there is continuous activity, but the set does not turn ON, this means that the EEPROM is not acknowledging the main micon"s request.

NOTE: This applies to ANU-1 and 2 chassis only. On the AP and FN-1 chassis, if the main micon does not receive acknowledgement from the EEPROM, it will revert back to the "preset" adjustments stored in the main micon's ROM.

Must Haves to Check First

1. Power
2. Ground
3. Master Clock
4. Reset
5. Vertical blanking (ANU-1 & 2, AP, and FN-1 chassis)

NOTE: Data and Clock must be 4.5 Vp-p or greater. Acknowledge and stop bits should be visible. Confirm waveshape for rise time.

Observations

- The tuner is not controlled via the I^2C bus. Do not confuse tuning problems with I^2C control problems. Likewise, the character generator is not part of the I^2C bus.
- It is easy to confuse I^2C bus problems with other problems which may cause the video to be muted, i.e. vertical failure and IK problems.

If the audio unmutes and is controllable the I^2C bus is operating. A problem may still exist with one of the slaves.

- Handshaking must occur for the unit to operate properly.

i.e. If one of the slaves does not behave properly, any number of symptoms may be experienced. Also pay particular attention to the video switcher IC since this interfaces with the outside world.

There are several zener diodes used on the data and clock lines. They are used to protect the bus from transients. Generally, there will be a set for each board. One failure mode is for the zener to become slightly leaky. This often does not significantly reduce the peak to peak amplitude of the data or clock. Instead, it tends to round the corners of the data or clock. You need at least 100 mhz bandwidth to observe this.

The symptom is one or more (possibly all) functions will not work correctly. Troubleshoot by lifting the zeners one at a time. Generally, this is best done by lifting the pair found on each board. Start with the A/V switch and dynamic convergence boards since these have had the most reported problems.

The data switch is used to disconnect the slaves from the I^2C bus during standby. The ANU-1 and 2 chassis use only one data switch, the AP and FN chassis use several. If the data switch(es) become leaky, this can cause numerous problems. Some of them are:

- One or more functions are inoperative or functions operate erratically.
- Unit will only power ON from the remote. All other functions operate correctly. Do not confuse this with the reset problem described in service bulletin CTV-40.

Items to Remember

It is important to remember what the jungle IC requires to develop horizontal and vertical drive. A failure here can easily be confused with I^2C problems:

- Horizontal drive from the Y/C jungle IC.
  NOTE: Requires about 9Vdc. Does not require I^2C input.
- Vertical drive from the jungle IC.
  NOTE: Requires about 9Vdc and correct I^2C input.
- Vertical Blanking from the Jungle IC. Used to time data transfer, etc.
  NOTE: Requires about 9Vdc. Does not require I^2C input.

The "M" bus used on the LN-1 chassis is similar in operation to I^2C. However, since the data density on the bus is much lower the only time there is activity seen on the bus during normal operation is:

1. Power ON polling
2. Whenever a customer command is executed.

Conversely, the I^2C bus has a very high data density and activity is continuously seen on the bus.

EEPROM Replacement Procedure for ANU-1/ANU-2 Chassis

When the EEPROM must be replaced there are three possible methods which can be employed. Choose the one that best applies:

When Another Working Television - Similar Model - is Available

1. Remove ac power to the television.
2. Carefully remove the defective EEPROM. Set it aside in a static protected bag or foam (you may want it later).
3. Install an IC socket in place of the EEPROM.
4. Remove the EEPROM, from the working unit, and install it into the IC socket.
5. Apply ac power to the television. If the set turns ON turn power OFF the set using the remote or front panel power button.

NOTE: When the set is plugged in, the main micon is reset. As part of it's housekeeping program, it fetches the adjustment data stored in the EEPROM and loads it into t's internal RAM. As long as ac power is applied and standby power supply operates, the data fetched from the ROM will be retained in the main micon's RAM.

6. Carefully remove the EEPROM (the good one in the IC socket) and install the new (unprogramed) replacement EEPROM in its place.

BE CAREFUL ! The set is plugged into the ac line and is powered-up in the standby mode.

7. While depressing the service switch, on the back of the unit, turn power ON using the remote or front panel power button. This will put the television in the service mode.

8. When the set comes on, use the remote to write all the adjustment data stored in the main micon's RAM into the replacement EEPROM. **NOTE:** To write the data, press the "MUTE" button followed by the "ENTER" button on the remote control. The screen should display the word "WRITE" in yellow. It will then change to red when the "ENTER" button is pressed.

9. Remove ac, to the television, wait 3 seconds then re-apply ac. The CPU will reset and fetch all the adjustment data stored in the EEPROM.

10. Check all functions and touch up adjustments as needed. (Don't forget to check the MTS functions.)

When the EEPROM Partially Functions

1. Remove the ac from the television.

2. Carefully remove the original EEPROM. Set it aside in static protected bag or foam.

3. Install an IC socket.

4. Install the original EEPROM into the socket.

5. Re-apply ac to the television and turn power OFF using the remote or front panel power button, if the set turns on. **NOTE:** When the ac is restored, the main micon is reset. As part of it's housekeeping program, it fetches all the adjustment data stored in the EEPROM and loads it into it's internal RAM.

6. Carefully remove the original EEPROM and install the new (unprogramed) replacement EEPROM.

BE CAREFUL ! The set is plugged into the ac line and is powered-up in the standby mode.

7. While depressing the service switch on the back of the unit, power ON using the remote or front panel power button. This will put the television in the service mode.

8. When the set comes on, use the remote to write all the adjustment data stored in the main micon's RAM into the EEPROM. To writ the adjustment data press MUTE, then ENTER. The screen should display the word "WRITE" and then change color (red) when ENTER is pressed.

9. Unplug the television, from the ac line, and wait 3 seconds. Plug it back in. The main micon will reset and fetch all the adjustment data stored in the EEPROM.

10. Check all functions and touch up adjustments as needed. (Don't forget to check the MTS functions.)

EEPROM is Dead and Another Working Television is not Available.

1. Replace the EEPROM.

2. Apply ac power and power up the set.

3. Enter the service mode and make adjustments as needed or enter the default values and fine tune the adjustments from that point.

NOTE: Don't forget to check the MTS adjustments.

4. If the set will not power up, it will be necessary to write some data into the EEPROM. To do this:

   a. While depressing the service switch, apply ac power to the set. While still holding in the service switch, depress the power switch on the front panel of the television (You can also use the remote control to turn power ON).

At this point even if there is no picture and the power supply has not been activated the CPU thinks that it is in the service mode.

   b. Push the "3" button on the remote eight or nine times. Next press the "MUTE" button. Finally, press the "ENTER" button.

NOTE: This will load some data into the "Horiz. Osc." adjustment location.

   c. Remove ac power to the television. Wait three seconds. Re-apply ac power and turn power ON. The unit should now come ON.

   d. Re-enter the service mode and make the necessary adjustments.

EEPROM Replacement Procedure for the AP/FN-1 Chassis

There are three methods that can be used:

When Another Working Television - Similar Model - is Available

1. Follow the same steps outlined for the ANU-1/ANU-2 chassis.

NOTE: The EEPROM is located on the Y2 board. An extender jig for this board makes the job much easier.

When the EEPROM Partially Functions

1. Follow the same steps outlined for the ANU-1/ANU-2 chassis.

NOTE: The EEPROM is located on the Y2 board. An extender jig for this board make the job much easier.

EEPROM dead - another model not available.

1. Unplug the television and install an extender jig for the Y2 board.

2. Carefully remove the original EEPROM and install a socket in its place.

3. Power up the television (Y2 board is extended and the EEPROM is removed).

The unit will automatically default to the adjustment data stored in the main micon's ROM.

4. Turn the television OFF using the remote or front panel control (it is plugged in).

5. Carefully install a replacement EEPROM into the socket.

BE CAREFUL ! The set is plugged into the ac line and is powered-up in the standby mode.

6. While depressing the service switch on the back of the television turn power ON using the remote or front panel control. This will place the unit in the service mode.

7. When the set comes ON use the remote to write all the adjustment data stored in the main micon's RAM into the EEPROM.

NOTE: To write the data into the EEPROM press the "MUTE" button followed by the "ENTER" button on the remote. The screen should display the word "WRITE" and then change color (red) when "ENTER" is pressed.

8. Remove ac power to the television and wait 3 seconds. Re-apply ac power. The main micon will reset and fetch all the adjustment data stored in the EEPROM.

9. Check all functions and touch up adjustments as needed. Don't forget to check the MTS functions.

Entering the Service Mode

To enter the service mode:

- Connect the set to the ac line.
- Press "Display" → "5" → "Volume +" → "Power" in sequence and within 0.5 seconds of each other using the Sony remote control.

Operation of the remote control buttons while in the service mode:

"1", "4"	Up/Down.	Selects the service item.
"3", "6"	Up/Down.	Changes the data for the service item.
"MUTING" → "ENTER"		Writes the data to the service item register. *WARNING! THIS CANNOT BE UNDONE.*
"0" → "ENTER"		Reads the service data from the EEPROM.
"8" → "ENTER" *		Sets all user controls to the factory settings (clears all user settings).

*** You must also exit the service mode by pressing the "8" → "ENTER" button combination when the set's ID code is changed.**

Model ID Codes

Model	ID-0		ID-1		ID-2		ID-3		ID-4	
KV27TS29(U)	64	1000000	127	1111111	64	1000000	0	0000000	16	0010000
KV27TS29(C)	64	1000000	127	1111111	0	0000000	0	0000000	16	0010000
KV27TS32(U)	127	1111000	127	1111111	104	1101000	0	0000000	16	0010000
KV27TS36(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000
KV27TS36(C)	120	1111000	127	1111111	8	0001000	64	1000000	16	0010000
KV27TW77(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000
KV27TW78(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000
KV32TS36(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000
KV32TS36(C)	120	1111000	127	1111111	8	0001000	64	1000000	16	0010000
KV32TS46(U)	120	1111000	127	1111111	72	1001000	36	0100100	16	0010000
KV32TS46(C)	120	1111000	127	1111111	8	1001000	36	0100100	16	0010000
KV32TW77(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000
KV32TW78(U)	120	1111000	127	1111111	72	1001000	64	1000000	16	0010000

Feature ID Codes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
ID-0	A/V 1	A/V 2	A/V 3	A/V 1-S	A/V 2-S	A/V3-S	MONITOR
ID-1	COMB FILTER	SPEAKER SW	VARIABLE / FIXED AUDIO OUT	BALANCE	TREBLE / BASS	SURROUND	MTS
ID-2	CLOSED CAPTION	SPANISH	AUDIO EQ	VIDEO LABEL	NT/NR/VM	TRINITONE	IR H.P.
ID-3	1 TUNER PIP	2 TUNER PIP	2 TUNER MPX-0	2 TUNER MPX-1	ANT SWITCH-1	ANT SWITCH-2	PAL/M,N
ID-4	FRENCH	PORTUGAL	ENGLISH	DGC CONTROL	DSP	FM RADIO	LUMIPON

AA-1 Chassis Adjustment Item List

No	Item	Disp.	Data Range	Adj / Fixed	Initial
1	AFC Loop Gain	AFC	0 - 3	Fixed: 0	0
2	H Frequency	HFRE	0 - 127	Adj	47
3	V Frequency	VFRE	0 - 31	Adj	18
4	V Center	VPOS	0 - 31	Adj	25
5	V Size	VSIZ	0 - 63	Adj	10
6	V Linearity	VLIN	0 - 15	Adj	8
7	V Correction	VSCO	0 - 15	Adj	6
8	H Center	HPOS	0 -15	Adj	6
9	H Size	HSIZ	0 - 31	Adj	16
10	Pin Amp	PAMP	0 - 31	Adj	22
11	Corner Pin	CPIN	0 - 7	Adj	3
12	Pin Pha	PPHA	0 - 15	Adj	8
13	V Compensation	VCOM	0 - 7	Fixed: 2	2
14	Green Amp	GAMP	0 - 31	Adj	20
15	Blue Amp	BAMP	0 - 31	Adj	19
16	G Cut OFF	GCUT	0 - 15	Adj	7
17	B Cut O	BCUT	0 - 15	Adj	7
18	Chroma Trap	CROM	0 - 63	Fixed: 28	28
19	Sub Contrast	SPIX	0 - 63	Adj	24
20	Sub Hue	SHUE	0 - 63	Adj	28
21	Sub Color	SCOL	0 - 63	Adj	30
22	Sub Brightness	SBRT	0 - 63	Adj	34
23	RGB Picture	RGBP	0 - 63	Fixed: 10	10
24	Sharpness	SHAP	0 - 15	Fixed: 7	7
25	V Pull in Ra	VSMO	0 - 1	Fixed: 0	0
26	Reference Line	REF	0 - 3	Fixed: 2	2

● Set up Value

AA-1 Chassis Adjustment Item List Continued

27	Red Out	ROFF	0 - 1	0 •	1
28	Green Out	GOFF	0 - 1	0 •	1
29	Blue Out	BOFF	0 - 1	0 •	1
30	ABL Mode	ABLM	0 - 1	Fixed: 0	0
31	Notch ON/OFF	NOTC	0 - 1	Fixed: 1	1
32	OSD Intensity	DRGB	0 - 1	Fixed: 0	0
33	V Angle	VANG	0 - 63	Fixed: 0	0
34	Display Position	DISP	0 -63	Adj	63
35	Sub Volume	SVOL	0 - 15	Fixed: 0	0
36	Sub Balance	SBAL	0 - 15	Adj	7
37	Sub Bass	BASS	0 - 15	Fixed: 8	7
38	Sub Treble	TRE	0 - 15	Fixed: 7	7
39	Upper Y Bow	UYBO	0 - 63	Adj	31
40	Lower Y Bow	LYBO	0 - 63	Adj	25
41	H Amp	HAMP	0 - 63	Adj	33
42	H Tilt	HTIL	0 - 63	Adj	33
43	Upper C Bow	UCBO	0 - 63	Adj	38
44	Upper Tilt	UTIL	0 - 63	Adj	40
45	Lower C Bow	LCBO	0 - 63	Adj	41
46	Lower Tilt	LTIL	0 - 63	Adj	46
47	DC Shift	DCSH	0 - 63	Adj	37
48	Pin P H Position	PHPO	0 - 127	Adj	76
49	Pin P Hue	PHUE	0 - 31	Fixed: 0	0
50	Model ID	ID-0	0 - 127	Adj	120
51	Model ID	ID-1	0 - 127	Adj	127
52	Model ID	ID-2	0 - 127	Adj	64
53	Model ID	ID-3	0 - 127	Adj	0
54	Model ID	ID-4	0 - 127	Adj	16

• Setup Value

AA-1 Chassis Factory Default Settings List

Power	On
TV / Video (Main Picture)	TV
CATV / Air	Cable
Last Channel	Ch 6 / Normal, Ch 3 / Aux
MTS / Stereo	Main
Channel Display	Off
Surround	Off
Volume	33%
Picture	100%
Hue	50%
Color	50%
Brightness	50%
Sharpness	50%
Treble	50%
Bass	50%
Balance	50%
Skip Memory	Ch 2 thru 13 / Normal, Ch 2 thru 6 / Aux
Speaker	On
Variable Audio Out	Variable
Channel Caption	Off (Clear)
Video Label	Reset
PIP Mode	On (1/9 Size)
PIP Position	Right Down
PIP TV / Video	TV
PIP Last Channel (Only 2 Tuner)	Ch 2
Closed Caption / Text	Off
Dual Language	English

AA-1 Board Adjustment Notes

The AA-1 chassis has been designed to be easily adjusted and repaired. Depending on the repair made, when the repair is done, some adjustment must be made. The following information is included to aid the technician as to the adjustments that are to be performed if the listed IC is replaced.

IC Replaced	**Necessary Adjustments**
IC101 Main Micon	DISP
IC102 EEPROM	Rough adjust, Set ID, HFRE, VFRE, SPIX, SHUE, SCOL and DISP.
IC301 Y/C Jungle	HFRE, VFRE, SPIX, SHUE and SCOL.
IC606 9 Volt Regulator	SPIX, SHUE and SCOL.

Rough Adjust: Rough adjust data can be entered into the new IC using the initial data listed in the "Item of Adjustments List", in the service manual, for the TV model being repaired.

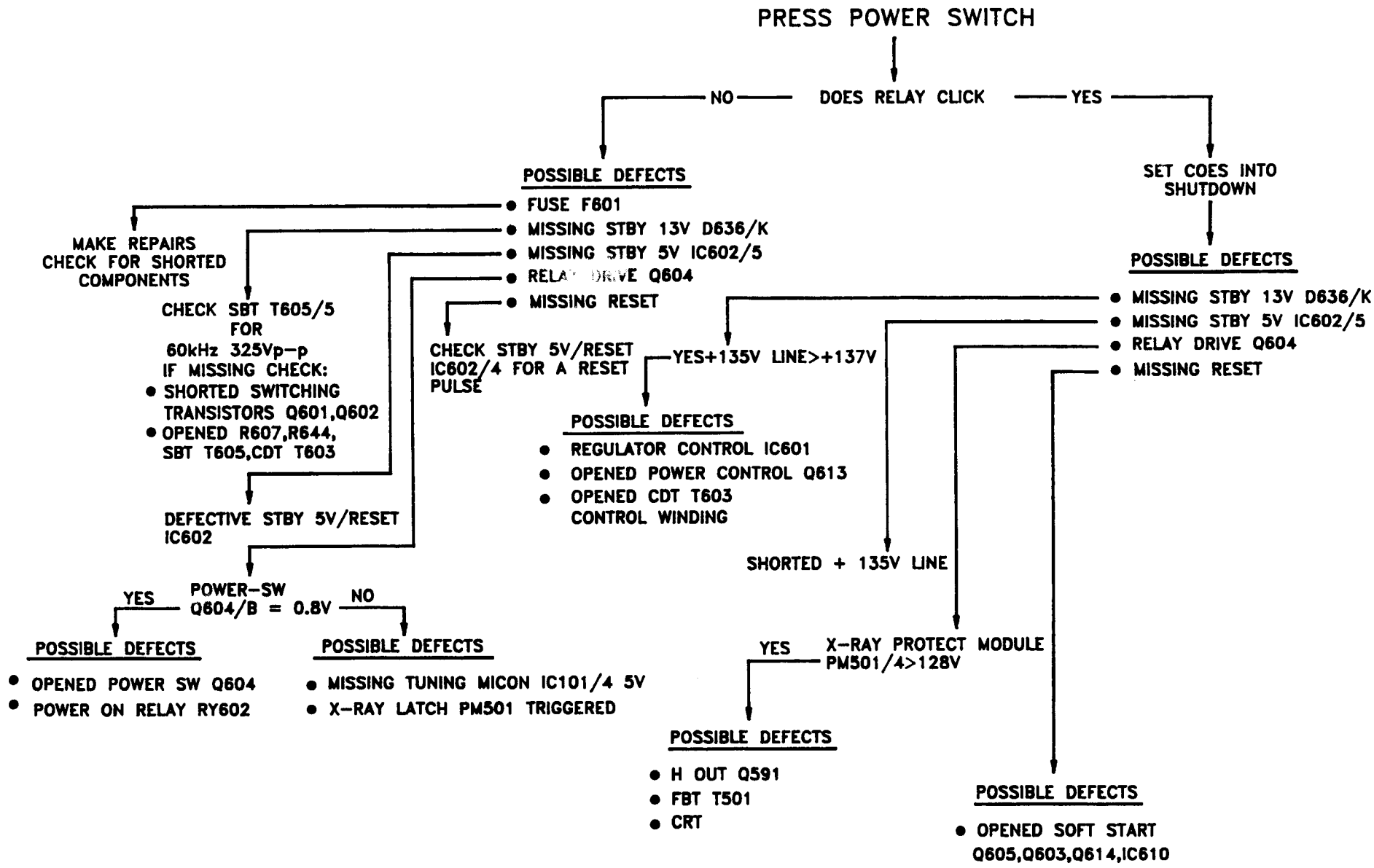
Set ID: Enter the model identification code, in the service manual, for the set being repaired.

AA-1 Chassis IC List

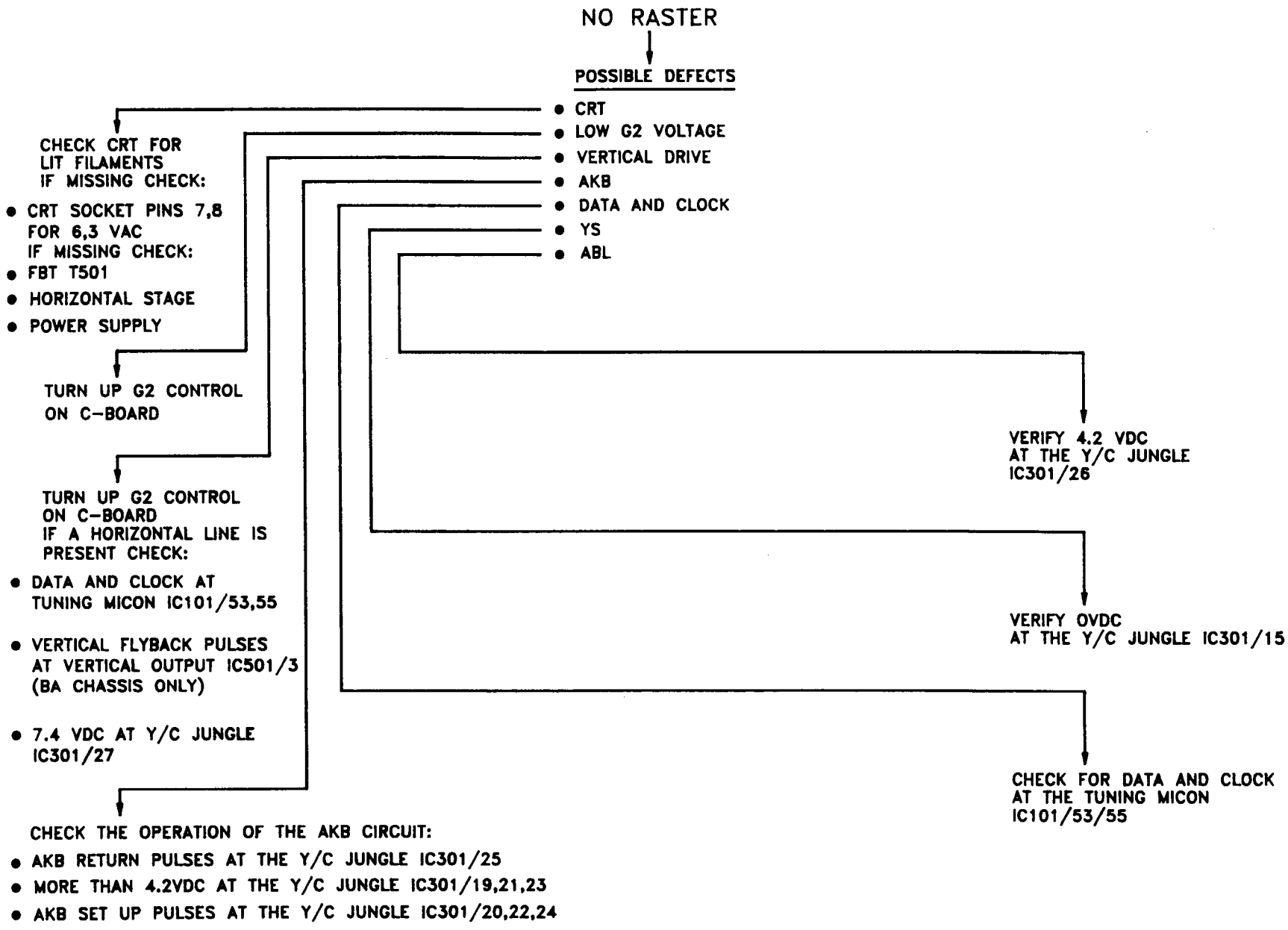
IC Number	Name	Description	Board	Part No.
IC101	Main Micon	CXP80424-065S (Sony)	M	8-752-841-16
IC102	Non volatile Memory	ST24C02AB1 (SGS Thomson)	M	8-759-043-86
IC150	Closed Caption Decoder	MC144143 (Motorola)	M	8-159-084-28
IC171	PIP Selector	CXA1315M (Sony)	A	8-752-058-68
IC172	Video Switch	BU4053BF (ROHM)	A	8-759-932-67
IC201	Audio Processor	TDA8424 (Philips)	M	8-759-090-21
IC201	Variable Audio Output Amplifier	LM358PS-T1 (National Semiconductor)	M	8-759-983-70
IC301	Y/C Jungle	CXA1465AS (Sony)	M	8-752-059-67
IC401	A/V Switch	M52470AP (Mitsubishi)	UA	8-759-637-10
IC402	A/V Switch with PIP	CXA1545AS (Sony)	UA	8-752-062-86
IC403	C Switch	MM1114XFF (Mitsumi)	UA	8-759-088-00
IC404	Y Switch	MM1118XFF (Mitsumi)	UA	8-759-164-18
IC501	Vertical Output	TDA8172 (Philips)	D	8-759-980-58
IC504	Pincushion Output	UPC393C (NEC)	D	8-759-106-93
IC601	Power Module	DM-48 (Sony)	D	1-810-051-11
IC602	Standby 5 Volt Regulator	L78LR05D-MA (Sanyo)	D	8-759-805-37

AA-1 Chassis IC List Continued

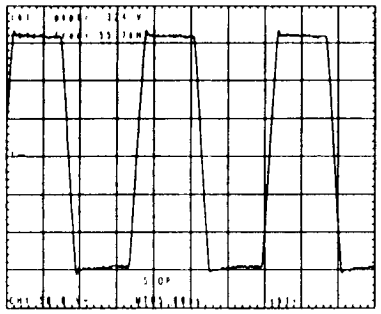
IC Number	Name	Description	Board	Part No.
IC604	5 Volt Regulator	LM7805CT (National Semiconductor)	D	8-759-924-12
IC605	12 Volt Regulator	LM7812CT (National Semiconductor)	D	8-759-929-62
IC606	9 Volt Regulator	MC7809CT (Motorola)	D	8-759-030-99
IC610	Inrush Control	UPC78L05JTP (NEC)	D	8-759-111-36
IC1001	SIRCS Sensor	SBX1618-51 (Sony)	D	8-741-100-62
IC1501	Dynamic Convergence Processor	CXA1526P (Sony)	E	8-752-052-88
IC1502	9 Volt Regulator	MC7809CT (Motorola)	E	8-759-030-99
IC1504	Dynamic Convergence Amplifier	LM358P (Texas Instrument)	E	8-759-903-58
IC2200	Audio Amplifier	TDA2009A (SGS Thomson)	D	8-759-980-43
IC3200	PIP Memory	MB81461B (Fujitsu)	P	8-759-971-56
IC3201	PIP Controller	MB86144 (Fujitsu)	P	8-759-093-2
IC3202	PIP A/D and D/A Converter	MB40176PF (Fujitsu)	P	8-759-093-28
IC3203	PIP A/D and D/A Converter	MB40176PF (Fujitsu)	P	8-759-093-28
IC3204	PIP Analog Processor	MB3512PF (Fujitsu)	P	8-759-093-26
IC3205	Inverter PIP Position	TC7SU04F-TE85L (Toshiba)	P	8-759-243-21



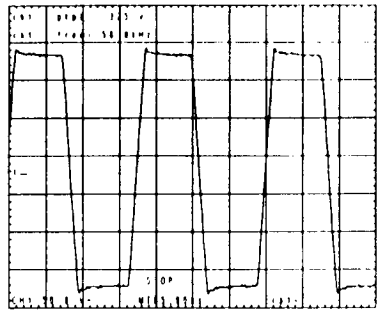
AA-1 POWER SUPPLY TROUBLESHOOTING FLOW CHART


NO RASTER
POSSIBLE DEFECTS
• CRT
• LOW G2 VOLTAGE
• VERTICAL DRIVE
• AKB
• DATA AND CLOCK
• YS
• ABL
CHECK CRT FOR LIT FILAMENTS IF MISSING CHECK:
• CRT SOCKET PINS 7,8 FOR 6,3 VAC IF MISSING CHECK:
• FBT T501
• HORIZONTAL STAGE
• POWER SUPPLY
TURN UP G2 CONTROL ON C-BOARD
TURN UP G2 CONTROL ON C-BOARD IF A HORIZONTAL LINE IS PRESENT CHECK:
• DATA AND CLOCK AT TUNING MICON IC101/53,55
• VERTICAL FLYBACK PULSES AT VERTICAL OUTPUT IC501/3 (BA CHASSIS ONLY)
• 7.4 VDC AT Y/C JUNGLE IC301/27
CHECK THE OPERATION OF THE AKB CIRCUIT:
• AKB RETURN PULSES AT THE Y/C JUNGLE IC301/25
• MORE THAN 4.2VDC AT THE Y/C JUNGLE IC301/19,21,23
• AKB SET UP PULSES AT THE Y/C JUNGLE IC301/20,22,24
VERIFY 4.2 VDC AT THE Y/C JUNGLE IC301/26
VERIFY OVDC AT THE Y/C JUNGLE IC301/15
CHECK FOR DATA AND CLOCK AT THE TUNING MICON IC101/53/55

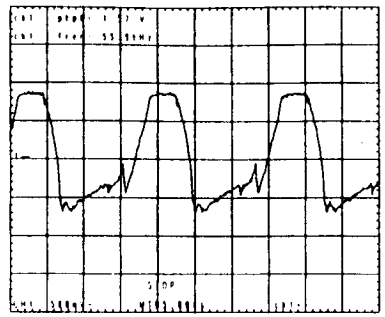
AA-1 NO RASTER TROUBLESHOOTING FLOW CHART



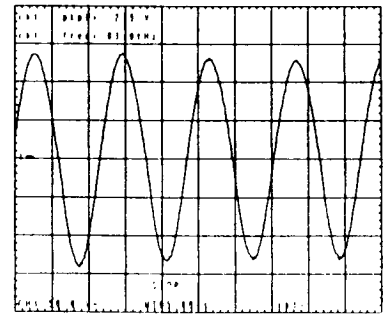
STANDBY Q601/B
50V/DIV. 5 μSEC. TB.



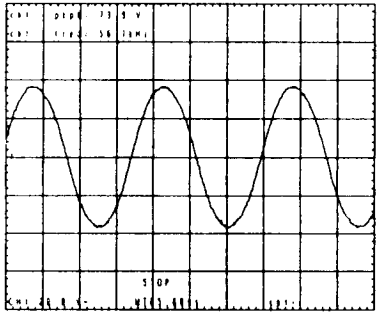
STANDBY T603/3
50V/DIV. 5 μSEC. TB.



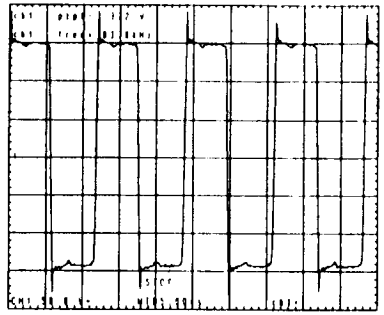
STANDBY Q602/B
500MV/DIV. 5 μSEC. TB.



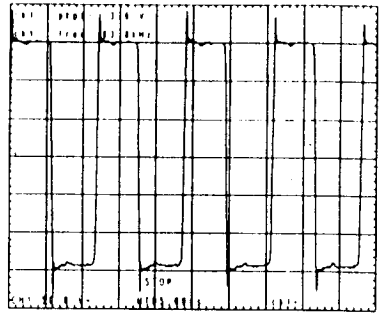
STANDBY T604/15
50V/DIV. 5 μSEC. TB.



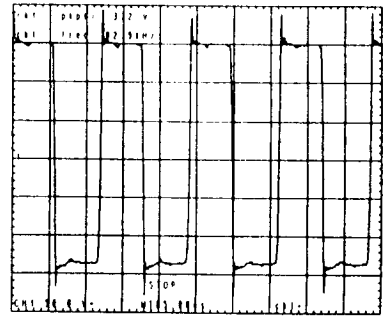
STANDBY T605/2
20V/DIV. 5 μSEC. TB.



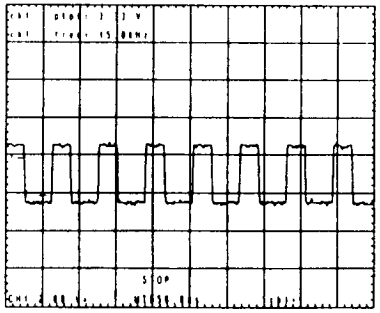
POWER ON Q601/E
50V/DIV. 5 μSEC. TB.



POWER ON T603/6
50V/DIV. 5 μSEC. TB.

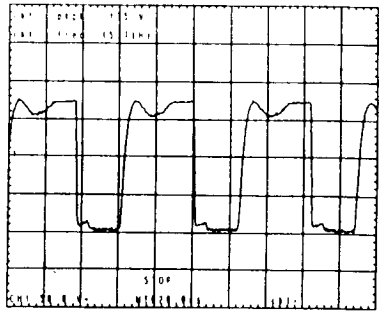


POWER ON T603/3
50V/DIV 5 μSEC. TB.

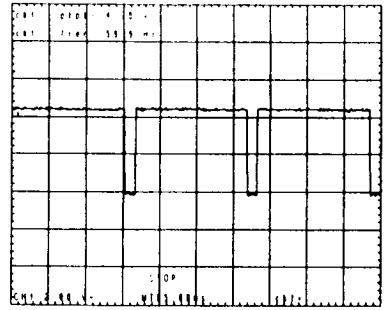


HORIZONTAL DRIVE Q502/B
2V/DIV. 50 μSEC. TB.

HORIZONTAL OUTPUT Q591/C
50V/DIV. 20 μSEC. TB.

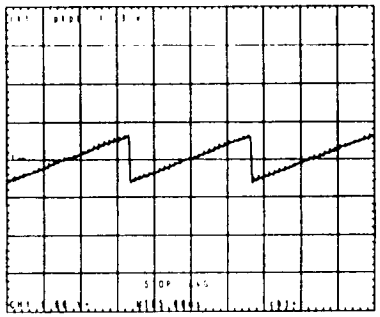


HORIZONTAL DRIVE Q502/C
50V/DIV. 20 μSEC. TB.

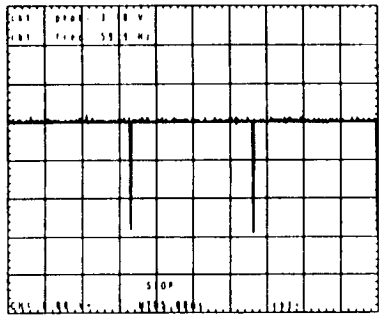


Y/C JUNGLE IC301/28 (V.VLK)
2V/DIV. 5MSEC. TB.

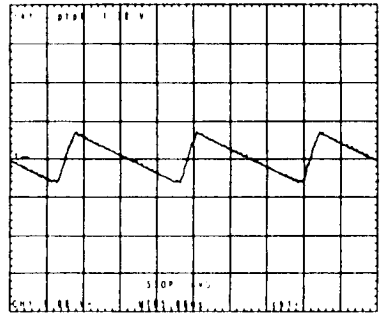
(continued)



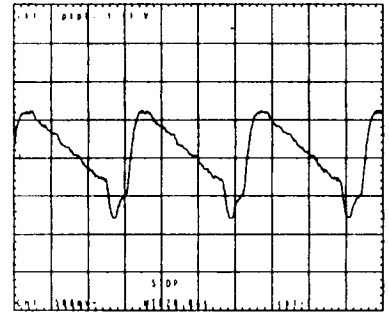
Y/C JUNGLE IC301/31 (V.DRIVE)
1V/DIV. 5MSEC. TB.



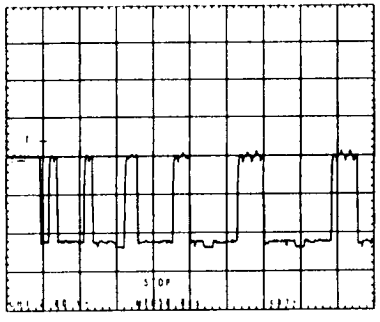
Y/C JUNGLE IC301/29 (V.PULSE)
1V/DIV. 5MSEC. TB.



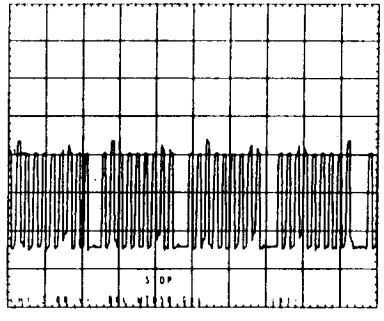
Y/C JUNGLE IC301/34 (V.OSC)
1V/DIV. 5MSEC. TB.



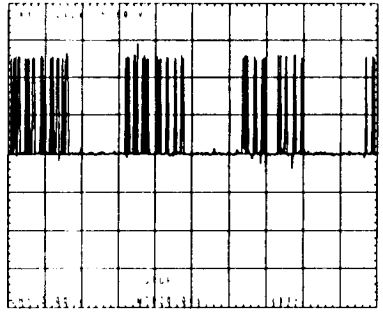
Y/C JUNGLE IC301/44 (V.SYNC)
500MV/DIV. 20 μSEC. TB.



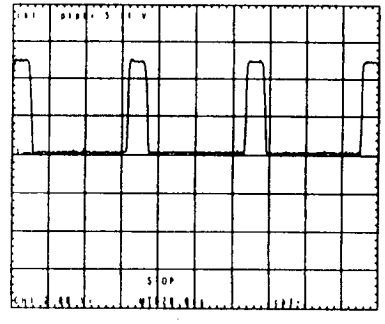
IC301/48 (SDL)
2V/DIV. 50 μSEC. TB.



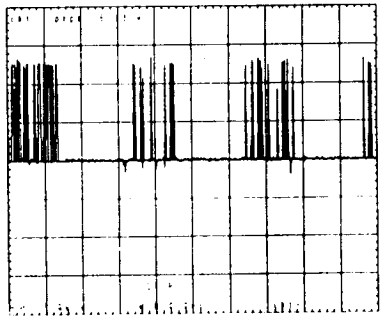
Y/C JUNGLE IC301/47 (SCL)
2V/DIV. 50 μSEC. TB.



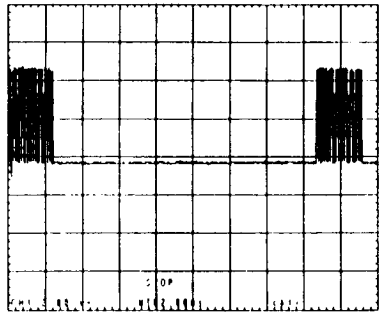
CLOSED-CAPTION IC150/4 (LUM)
2V/DIV. 20 μSEC. TB.



CLOSED-CAPTION IC150/8 (HP)
2V/DIV. 20 μSEC. TB.

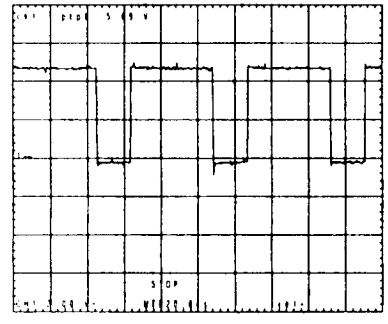


CLOSED-CAPTION IC150/7 (BLUE OUT)
2V/DIV. 20 μSEC. TB.



CLOSED-CAPTION IC150/3 (BOX)
2V/DIV. 2MSEC. TB.

CLOSED-CAPTION LINE 21 FIELD 1
200MV/DIV. 10 μSEC. TB.



CLOSED-CAPTION IC150/3 (BOX)
EXPANDED VIEW
2V/DIV. 20 μSEC. TB.